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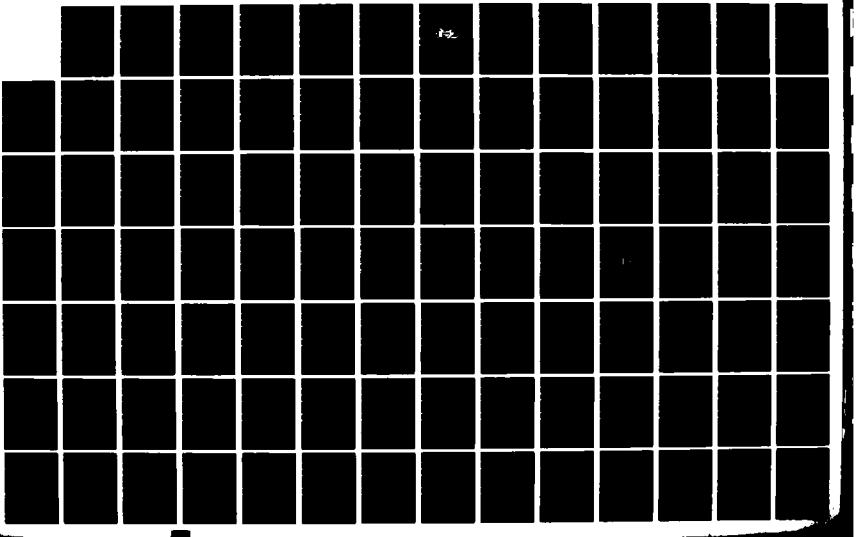

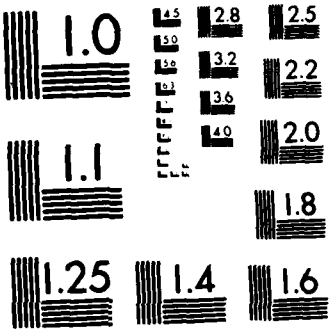

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PNPN LATCHUP IN BIPOLAR LSI DEVICES

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20 ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

PNPN latchup was studied both analytically and experimentally in several bipolar LSI technologies including integrated injection logic (I^2L), integrated Schottky logic (ISL), Schottky Transistor logic (STL) and emitter coupled logic (ECL). The latchup analysis procedure was expanded and applied to LSI microcircuits representing each of the technologies. This procedure consists of, a) the identification of parasitic PNPN paths, b) the electrical characterization of the paths, c) detailed circuit analysis, and

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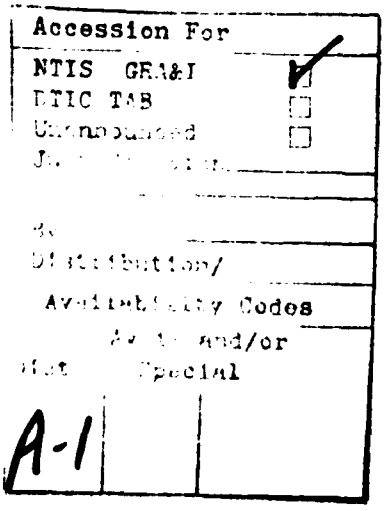
20. ABSTRACT (Continued)

d) determination of worst case bias conditions for radiation testing. The identification was performed from chip photomicrographs and composite mask drawings. The characterization was performed experimentally by measuring parasitic transistor gains and SCR parameters on decoupled paths and analytically by using a semiconductor device physics code (PN code) in conjunction with doping profiles. The detailed circuit analysis was performed either by hand or with the circuit analysis code SPICE. Radiation testing was performed at the White Sands Missile Range LINAC facility.

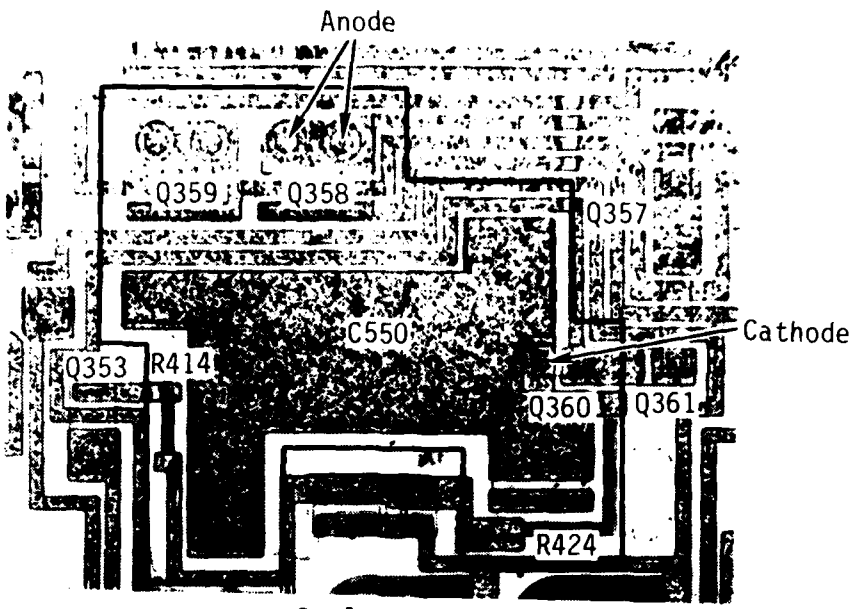
The results of the study were, a) latchup cannot occur in non-isolated I^2L, b) latchup cannot occur in the internal logic of ISL or STL without causing a problem with electrical performance, c) no latchable paths were found by analysis in the 93471 ECL 4K RAM, the I/O buffers on an ISL/STL gate array or the I^2L peripherals of the 9408 I^3L microprogram sequencer. The radiation tests confirmed the analysis, and d) a PNPN path was found in the I^2L AD571 10 bit A/D converter which would latch in circuit simulations. However, none of the test samples could be latched under radiation.



SUMMARY

In this report a latchup analysis procedure developed for bipolar microcircuits, has been expanded and applied to several bipolar LSI circuits including a microprocessor, a microprogram sequencer, 4K Static RAM, a 10 bit A/D converter and an ISL/STL gate array. It should be emphasized that a thorough application of the analysis procedure to a complex LSI array is not an easy task without the cooperation of the manufacturer. If one does not have access to a mask set, processing details, detailed circuit diagrams and doping profiles the task can be very tedious at best and can require a high power microscope, a failure analysis lab (with equipment for etching, angle lap and stain, microprobing, spreading resistance profiling) and access to circuit simulation and device physics computer codes. For some circuits, however, the task is greatly reduced. For non-isolated I^2L a simple circuit analysis is sufficient to prove that latchup cannot exist. For an ISL or STL array a simple circuit analysis is sufficient to show that if latchup did occur the circuit would not pass the electrical specifications. In the case of oxide separated technologies that utilize T^2L peripheral and I/O circuits all but substrate latchup can be dismissed by assuring that each individual component is surrounded by an oxide-sidewall. Since an increasing number of high density bipolar LSI circuits are being built with some form of oxide-sidewall technology the latchup analysis of future LSI circuits may indeed be somewhat trivial. However, as illustrated by the AD571, circuits which employ linear circuitry can require a very complex analysis and lead to inconclusive results. Although a thorough analysis of the AD571 indicated that latchup should occur either electrically or with radiation, the circuits could not be latched.

A possible explanation for the failure of the AD571 to exhibit latchup of the bipolar offset circuit may be due to the geometry of the parasitic PNPN path. As shown in the photomicrograph on the following page, the parasitic path between the emitter of Q358 and emitter of Q360 in the



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bipolar offset circuit is rather long. The separation between p regions (i.e. base width of lateral PNP) is ~250 μm. When current is forced to flow from anode to cathode in this path a latchup condition occurs. As stated previously the holding current for this path is 1.5 mA. The maximum gain of the lateral PNP was measured to be .008 and the gain of the NPN (Q360) was 210. However in the context of the actual circuit operation sustaining any current flow from the emitter of Q358 to the base of Q360 will be hampered by the large separation of these regions. Since the collector of Q358 completely surrounds the emitter it is unlikely that Q358 emitter current will be diverted to Q360 even under favorable bias conditions.

There are three possible categories of latchup vulnerability for integrated circuits.

1. Latchup cannot occur even under favorable bias conditions and/or process variations.
2. Latchup will always occur without major changes in design and/or processing.
3. Latchup may occur under certain bias and temperature variations but can be prevented by minor design and/or process variations.

Nonisolated I^2L fits in category 1 along with dielectrically isolated circuits where each component is fully dielectrically isolated. The junction-isolated oxide-sidewall technologies reported on in this paper fit in category 3. In the three examples studied it was shown that latchup could not occur in the internal arrays (I^2L, ECL memory cell and ISL/STL inverters) and that in the peripheral and I/O T^2L circuitry there were no multiple components within an isolation region except for the Darlington transistor pair on the 9408 (which has been shown to be latchup free). Therefore, the only possibility for latchup is with a parasitic PNPN path

through the substrate. Based on a first order relation for the gain of the lateral substrate NPN transistor, parametric curves were presented which can be used in the design of latchup free circuits.

The results of the latchup analysis of the AD571 indicated that latchup should occur. Yet none of the circuits tested could be latched either electrically or with radiation. From the initial analysis of the AD571 it would appear to fit into category 2. Over 200 distinct PNPN paths were identified and all could easily be latchup when decoupled from the circuit. However, after a detailed circuit analysis all but one of the paths could be eliminated because the bias conditions were not favorable for latchup or the path was actually functioning as an "on" SCR in the circuit with a controlled current. The one path which, according to the analysis, should have been latchup prone apparently failed to latch because of its geometrical configuration. Although from the experimental tests results, the AD571 is seemingly latchup free, the analysis of the technology indicates that the potential for latchup in junction-isolated linear circuitry is much greater than for oxide-sidewalled bipolar technologies.

In addition to the application of the latchup analysis procedure to specific LSI circuits, a considerable amount of work was performed to investigate techniques for analytically predicting parasitic transistor gains and holding currents and voltages. A hierarchy of modeling techniques was established depending on the application. For calculation of worst case gain products, first order closed formed expressions can be used. If the prediction of holding current is required, semiconductor device physics code calculations can be made of the gain vs emitter current for each parasitic transistor. If a complete definition of the current-voltage characteristics are required then the analytical technique must use a semiconductor device physics calculation of the PNPN path or a circuit model. Both approaches were investigated. It was concluded that a two transistor analog circuit can be used to calculate SCR I-V characteristics

if good transistor model parameters are available and certain precautions are taken. However, it was concluded that a one-dimensional device physics code calculation of the SCR characteristics is probably inadequate because of the two dimensional aspects of most parasitic PNPN paths.

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LIST OF ILLUSTRATIONS (Concluded)

1. INTRODUCTION

Four layer latchup is a phenomenon which can occur in integrated circuits because of the presence of parasitic PNPN paths which, if properly biased, may be triggered "on" by ionizing radiation. The usual results of this latchup are to prevent operation of the circuit until the power supply bias is reduced to a value low enough to break the latch. If current to the latch is not limited sufficiently damage may result. Latchup was first found in bipolar SSI circuits and has recently proven a major problem in bulk CMOS devices. A procedure has been developed for analyzing ICs to determine whether or not four layer latchup is probable and the procedure has been applied to several bipolar MSI and linear circuits[1,2]. In this report the latchup analysis procedure has been expanded and applied to several bipolar LSI devices which are representative of current bipolar LSI technologies. The technologies include both non-isolated and isolated Integrated Injection Logic (I^2L), linear compatible I^2L, isoplanar Emitter Coupled Logic (ECL), Integrated Schottky Logic (ISL) and Schottky Transistor Logic (STL). In addition to electrically characterizing certain PNPN paths to determine if they are latchable under worst case bias conditions, various paths were studied analytically to determine under what design and processing constraints the paths could be made latchup proof. After the analysis was completed, radiation tests were performed at various pulse widths and dose rates to verify the results of the analysis.

2. TECHNOLOGIES AND SPECIFIC DEVICES ANALYZED

In this study many current bipolar LSI technologies have been investigated for latchup through the analysis of specific devices. Table I is a list of these devices along with a circuit description and technology description.

TABLE I. LSI devices analyzed for latchup.

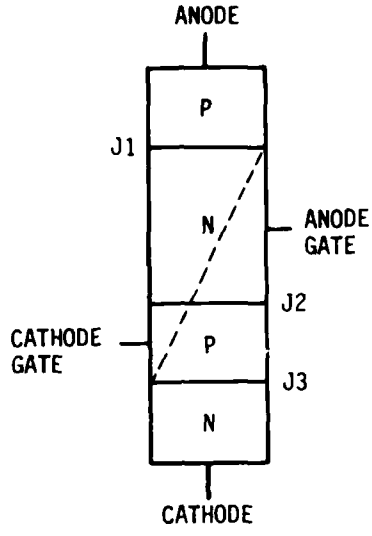
Device Type	Manufacturer	Description	Technology
SBP9900A	T.I.	16 bit microprocessor	non-isolated, oxide separated I^2L
9408A	Fairchild	microprogram sequencer	isoplanar, junction-isolated I^2L with T^2L peripheral and I/O
93471	Fairchild	4096 x 1 STATIC RAM	isoplanar, ECL memory cells, T^2L peripheral and I/O
AD571	Analog Devices	10 bit monolithic A/D converter	junction-isolated analog compatible I^2L with T^2L I/O
XXX	Harris	Special test device	ISL and STL test devices in junction-isolated polyplanar with T^2L I/O

The SBP9900A, 9408 and AD571 were chosen to represent the three major variations of I^2L currently in use. These are nonisolated I^2L where the outputs are open collector inverted transistors, isolated I^2L using I^2L for the internal logic and T^2L for the I/O, and linear compatible I^2L where analog and digital circuitry are combined on the same chip. In order to achieve very high density bipolar microcircuits most manufacturers are using some form of oxide-sidewall technology. This allows closer spacing of components and, by using the oxide sidewalls as diffusion stops, allows much smaller diffusion and/or implant areas. Oxide-sidewalls are used in all of the circuits investigated in this study except for the AD571. Although there are no ISL/STL devices currently on the market (with the exception of a gate array) this technology was investigated in the form of a test device from Harris which included both ISL and STL gates. Therefore, the comments on this technology are preliminary.

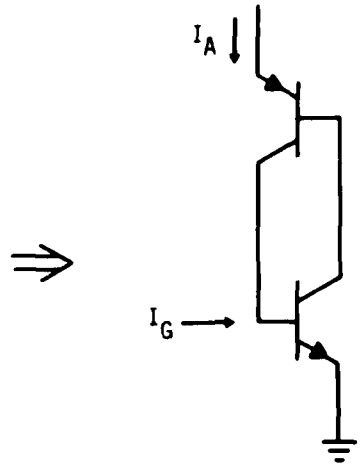
3. LATCHUP ANALYSIS PROCEDURE

An analysis procedure for determining the probability of four layer latchup occurring in a bipolar integrated circuit was developed several years ago[1]. This procedure is currently being formalized and presented to ASTM committee F-1 as a guide for latchup analysis[2]. This basic procedure has been utilized in this study and expanded where needed.

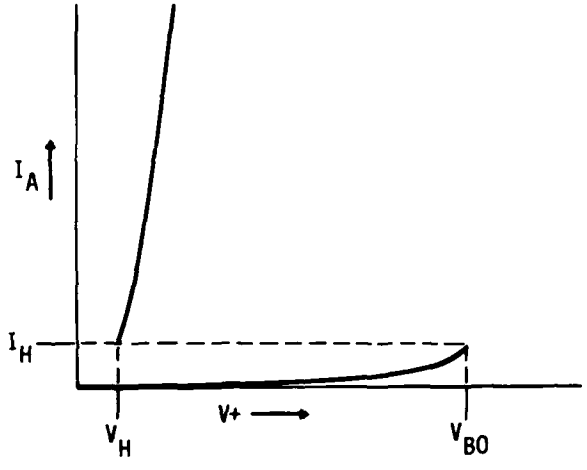
Four-layer latchup occurs in a microcircuit when a parasitic PNPN path is triggered into a low conductance state. The basic characteristics of four-layer latchup are illustrated in Figure 1. The terminology to be used throughout the report is given in Figure 1-a. The four layers are the anode, anode-gate, cathode-gate and cathode with junctions J1, J2 and J3. As shown in Figure 1-b, the PNPN structure can be represented by two merged transistors. The DC I-V characteristic of the path is shown in Figure 1-c for positive anode voltage with the gates open. When the positive voltage is large enough to avalanche J2, I_A reaches a value where the product of



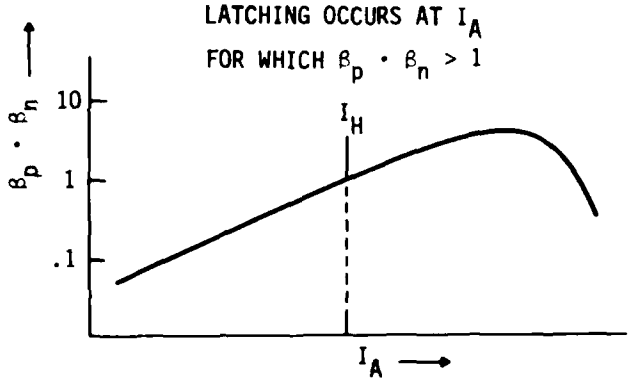
a.) Nomenclature for PNPN path.



b.) Two transistor analog of PNPN path.



c.) Positive voltage I-V characteristics.



d.) Current gain produce -vs current for PNPN path.

Figure 1. PNPN characteristics.

the common-emitter current gains of the the two parasitic transistors is one. At this point regenerative action occurs between the transistors and both are maintained in saturation. As illustrated in Figure 1-d, the minimum current for which this condition occurs is called the holding current, I_H. The anode-cathode voltage drop in the low conductance "on" state is the forward voltage drop on the PNP emitter-base junction plus the $V_{CE}(Sat)$ of the parasitic NPN, plus the IR drop through the PNP base region. The minimum voltage in the "on" state is the holding voltage, V_H. A PNPN path will not exhibit the low conductance state, i.e. will not latch, if the current gain product is less than one at all anode currents. Also the path will not sustain a latch if the current is limited to a value less than I_H or the voltage to a value less than V_H.

The latchup analysis procedure consists of three phases; identification, characterization and circuit analysis. A flow diagram illustrating this procedure is given in Figure 2.

3.1 IDENTIFICATION

In the identification phase all parasitic four layer paths on the LSI device are located. This can be done from a photomicrograph of the chip which details each component or from a composite overlay mask obtained from the vendor which identifies each diffusion or implant. When working from a photomicrograph it is important to understand the process such that each region can be identified. If the circuit uses two level metallization (as is the case for most bipolar LSI), then at least two detailed photomicrographs are required; one of the top surface metallization and one with the interlevel dielectric removed to expose the first level metal. It may also be necessary to remove all metal to clearly identify all implant/diffusion regions and contact openings. In the work presented in this paper all identification was performed from photomicrographs, usually at 250X. Another important aspect of the identification phase is establishing a circuit diagram. If a complete circuit diagram can be obtained from the

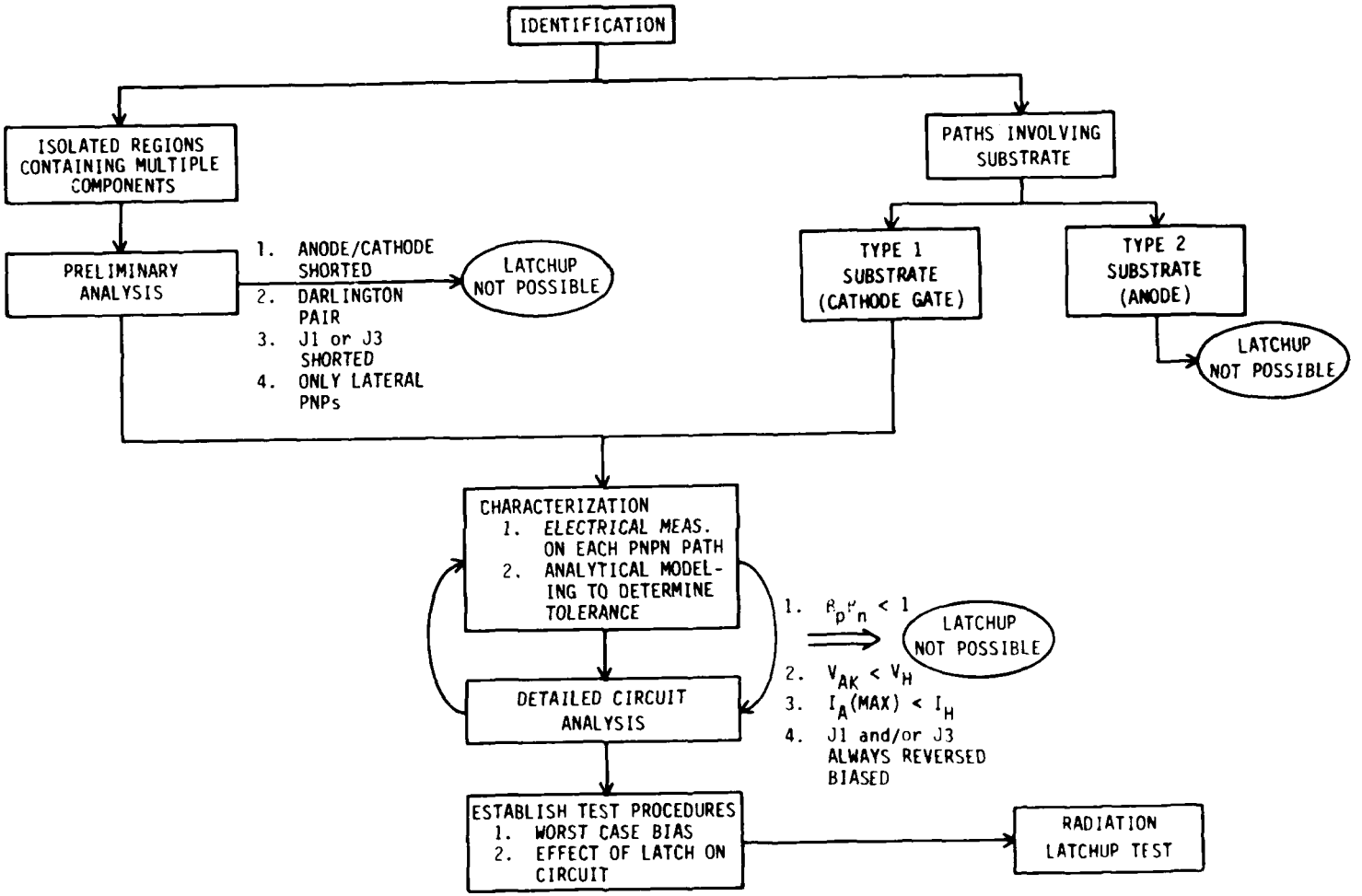


Figure 2. Flow diagram for latchup analysis.

vendor then it must be checked against the composite mask of photomicrographs. Otherwise it must be reconstructed from the chip photos or masks.

There are two types of PNPN paths which can occur in bipolar LSI circuits: those contained within an isolated region and those involving the substrate (including the P+ isolation diffusion on fully junction isolated devices). In fully dielectrically isolated parts the second type does not exist. The first step is to identify all isolated regions which contain multiple components (diodes, transistors and diffused resistors). Each parasitic PNPN path within these regions should be identified in the context of the circuit diagram. After identifying all PNPN paths a preliminary anlaysis can be performed to reduce the required characterization task. PNPN paths can be eliminated from further consideration if the anode and cathode are shorted, J1 or J3 are shorted, the path is within a Darlington transistor pair or the path occurs only between lateral PNP transistors.

There are two types of paths involving the substrate: a path with the substrate as the cathode-gate and a path with the substrate as the anode. For the case where the substrate is the anode, latchup cannot occur if the substrate is tied to the most negative potential in the circuit. Although during a dose rate environment sufficient current may flow in the substrate to raise the anode potential to a value greater than V_H with respect to the cathode, there is no current source to sustain a latch after the photocurrent subsides. However, in the case where the substrate is the cathode-gate, the normally reversed biased cathode-gate cathode junction, once forward biased by photocurrent, can be sustained if the shunt resistance to the actual ground (or V-) contact is sufficiently large. This will be discussed in more detail under the results section.

All of the PNPN paths which cannot be eliminated as latchup proof by the preliminary analysis are subjected to a detailed circuit analysis and

characterization. This is shown in the flow diagram as an interactive process since all of those paths eliminated by circuit analysis need not be characterized and those paths which are determined by characterization to be unlatchable need not be analyzed in their circuit configuration.

3.2 CHARACTERIZATION

The characterization phase involves both electrical measurements of the PNPN path totally isolated from the rest of the circuit and analytical modeling to determine what the first order layout and processing variables are that control the latchup characteristics of the path.

3.2.1 Electrical Characterization

In order to perform electrical measurements on the PNPN path all of the metallization interconnects to the four regions must be disconnected. This can be accomplished by capacitive discharge, laser scribing or, if there is a glassivation over the metal lines, by selectively cutting through the glass and etching away the metal beneath the cut. Once the path is isolated, the occurrence of latchup is determined by applying an increasing positive voltage on the anode with respect to the cathode using a curve tracer (with current limiting to the path to avoid burnout). If the path does exhibit latchup then the holding voltage and holding current should be recorded. If latchup does not occur then the path should be characterized analytically to determine what topological or processing parameter changes might make the path latchup susceptible.

3.2.2 Analytical Characterization

In past efforts on latchup analysis, the characterization phase has always been performed by taking a sample of the device type, (often a sample size of one) decoupling the leads and electrically determining whether

or not a path will latch. This totally empirical approach has been performed in two ways. First, the PNPN path in question is merely tested under worst case bias (gates open) to determine if the anode to cathode path is bistable. If the path does exhibit SCR action then I_H and V_H are recorded. The second approach is to not only measure the I-V characteristic but to also include measurements of β vs I_E on both the parasitic NPN and PNP transistors. By measuring the parasitic β's vs the emitter current, the maximum β_n, β_p product can be determined as well as the minimum current for which this product is equal to one. These measurements provide information which can be used to determine the margins for latchup susceptibility. If the path does latch then it can be determined how much the parasitic NPN or PNP gain must be degraded to prevent latchup, and if the path does not latch, then the amount of margin can be determined that will guarantee that the path will not latch. There are two major problems with this strictly empirical approach. First, without an analytical model to predict either the parasitic gains or the latchability of the path, one cannot predict when variations in the geometric or physical parameters of the process will result in a sufficient increase in the β product to cause latchup in a path that was determined to be latchup proof. The second problem is that the gain vs I_E values measured for the parasitic path may not be representative of the "effective" gain of the parasitic element in the actual PNPN path. This second point was the subject of a recent paper presented at the 1981 Nuclear and Space Radiation Effects Conference[3] and has been verified by this study. Because of the location of metal contacts to the various regions of the parasitic elements, the measured gain can be much lower than the effective gain. Therefore an analytical model is necessary to calculate "effective" gain.

In this study several analytical approaches have been investigated both to calculate effective parasitic gains and to predict latchup susceptibility of parasitic PNPN paths. The objectives of these analytical approaches are to be able to predict for a specific PNPN path whether or

not it will latch and then to determine the latchup susceptibility of the path when one or more geometric or physical parameters of the path are varied. By using the results of such an analytical approach, design and processing guidelines can be established to assure that specific PNPN paths will not latch in the context of their circuit configuration.

There are several methods to assure that a PNPN path will not latch in its circuit configuration. The easiest way is to assure that the product of the parasitic NPN and PNP βs is less than one at all current levels. Another approach is to assure that the holding current for the path is greater than the current limited to the path by the circuit or that the holding voltage is greater than the maximum potential that can occur between the anode and cathode.

If the first approach is chosen, that of assuring that $\beta_n \cdot \beta_p < 1$, then the easiest way to guarantee this relation is to assure that $\beta_n(MAX) \cdot \beta_p(MAX) < 1$. With this approach one does not need a model that predicts gain vs current but only the maximum value of gain at any current. Most first order, closed form analytical expressions for calculating gain are of this form. Thus, the simplest analytical approach is to use first order approximations based on a one dimensional analysis to predict parasitic gains. Such expressions can be found in semiconductor device physics textbooks[4],[5]. The problem with this approach is that the predicted gain given by these expressions is generally much greater than the "effective" gain in the actual PNPN path. Thus the simple approach usually gives a worst case analysis. The next level of sophistication in an analytical approach would be to use a one-dimensional semiconductor device physics code such as the PN code or SEDAN to calculate the gain vs current characteristic of the parasitic transistors. With this approach the actual $\beta_n \cdot \beta_p$ product can be predicted as a function of anode current and the holding current can be calculated. An even better approach would be to use a two or three dimensional code to calculate gains.

However, no readily available, multi-dimensional codes are available at present. The next higher level of analytical modeling of latchup susceptibility is to model the actual PNPN path. This can be done either with a circuit model or a semiconductor device physics model. In a circuit model, a two transistor analog of the SCR is modeled along with any parasitic resistances or capacitances present in the path. In order to effectively model the SCR with this approach, the model input parameters of each of the circuit elements must be known. In the semiconductor device physics model approach, a code capable of handling a four layer structure must be used. The ultimate analytical approach would be to use a multidimensional semiconductor device physics code capable of modeling a four layer structure.

Thus in approaching the modeling of a parasitic four layer path within a bipolar integrated circuit, there is a hierarchy of techniques available that can be chosen on the basis of how much information is necessary to define the latchup susceptibility of the path.

In Table II a list is given of the various modeling approaches in order of complexity along with the amount of information required to make the calculations and the information that can be determined.

In this study the approaches numbered 1, 2, 4 and 5 were investigated. Since no 2-d codes were available, approaches 3 and 6 were not attempted. The closed form approximations for gain calculations were taken from semiconductor device physics textbooks[4],[5] as well as from the work of Estreich.[6] The semiconductor device physics code utilized was the PN code.[7] This code was chosen not only because of availability and documentation but because it is capable of multilayer evaluation and has provisions for radiation effects inputs. The SPICE circuit analysis code[8] was chosen for the two transistor circuit analysis because of availability, ease of use and convenience of transistor models. Although in the SPICE-2E

TABLE II. List of modeling approaches.

	MODELING APPROACH	INPUT DATA REQUIRED	CHARACTERISTICS PREDICTED
1.	1-d closed form expressions	N_B, N_E, W_B, τ	$\beta_N(MAX)$, $\beta_p(MAX)$
2.	1-d code calculations	N(x), τ(x), μ(N)	$\beta_N(I_E)$, $\beta_p(I_E)$, I_H
3.	2-d code calculations	N(x,y), τ(x,y), μ(N)	$\beta_N(I_E)$, $\beta_p(I_E)$, I_H
4.	Circuit code calculations of PNPN	parasitic R, C, Model input parameters for Xstrs	I-V characteristic of SCR, I_H, V_H, t_{ON}
5.	1-d code calculations of PNPN	N(x), τ(x), μ(N)	I-V characteristics of SCR, I_H, V_H, t_{ON}
6.	2-d code calculatins of PNPN	N(x,y), τ(x,y), μ(N)	I-V characteristics of SCR, I_H, V_H, t_{ON}

version, used in this study, the transistor models do not have avalanche parameters, it is still possible to incorporate a breakdown model by including a diode with breakdown in junction J_2. This approach was developed by Bell Laboratories.[9]

3.3 DETAILED CIRCUIT ANALYSIS

The detailed circuit analysis is performed in order to determine whether or not the proper bias conditions can exist under worst case operating conditions to sustain a latch. The results of the detailed circuit analysis can be used to eliminate paths which meet certain criteria but it will generally not prove that latchup will indeed occur. PNPN paths can be eliminated from further consideration if a) $V_{AK} < V_H$, b) $I_A(MAX) < I_H$, or c) J1 or J3 are always reversed biased.

For those paths which cannot be eliminated by the above criteria, the circuit analysis should establish the worst case bias conditions under which the path is latchable and the observables at the external terminals if the path does latch. Once these are known, a radiation latchup test can be designed and performed.

4. RESULTS OF THE LATCHUP ANALYSIS

4.1 SBP9900A

In early radiation characterization studies on I^2L it was concluded that I^2L was latchup free[10,11]. This can be shown by circuit analysis. In Figure 3 a cross section of two single output I^2L gates fed by the same injector is shown for the SBP9900A process. There are two possible PNPN paths that can occur; one from the p type injector through an output and the other from the input of one gate through the output of

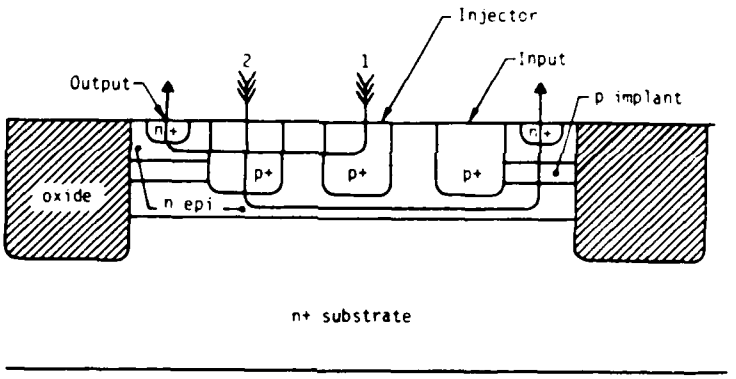


Figure 3. T.I. single output I^2 gates showing two types of PNPN paths.

another gate. In both cases the maximum voltage that can occur from the anode to the cathode is the forward diode drop between the p+ and n epitaxial layer minus the V_{CE}(Sat) of the inverted NPN transistor. This is due to the fact that the n epitaxial layer is always grounded. Since the holding voltage, V_H, for the path is the forward diode drop plus the NPN V_{CE}(Sat) the path cannot latch. Another way of reaching the same conclusion is to analyze the current in the path. Since the anode-gate (n epi) is grounded, current is from the anode and cathode to ground rather than from anode to cathode. Therefore latchup is not possible in nonisolated I^2L.

4.2 9408

The Fairchild 9408 is a junction isolated, isoplanar (oxide-sidewall) I^2L device using T^2L input and output circuitry. Since latchup is not possible within the I^2L array, the latchup analysis of the 9408 was reduced to an analysis of the I/O circuits and possible latchup paths through the substrate. The 9408 chip was photographed, the interlevel dielectric was removed and the chip was rephotographed. The inputs and outputs were studied in detail to determine if any isolation regions contained multiple components. The only isolated region containing more than

one device was a Darlington transistor pair in the output circuit. This configuration has been show to be latchup free in a previous analysis[1],[2]. Therefore, the analysis of the 9408 is reduced to an analysis of substrate latchup. As discussed in the section on the analysis procedure the only PNPN path involving the substrate which can be biased properly to allow for latchup is a path involving the substrate as the cathode gate. It has been argued[1],[2] that since this path is reverse-biased, when the substrate is held at the most negative potential in the circuit, substrate latchup cannot be sustained. A closer look at this path indicates that latchup may be possible under certain circumstances. This is illustrated in Figure 4 showing two adjacent NPN transistors in an isoplanar I/O circuit. The parasitic PNPN path is from the base region of one transistor through the substrate and out through the collector of an adjacent transistor. With no current in the substrate the potential on the cathode-gate is zero volts and J3 is reversed biased. However, under ionizing radiation a rathe. large photocurrent can occur in the substrate which may forward bias J3 and temporarily latch the PNPN structure if the anode to cathode bias is > V_H and $\beta_p \cdot \beta_N > 1$. Once the path is turned on J3 can be maintained in forward bias by the shunt resistance R_S between the cathode-gate and the substrate ground contact point. If the ground contact to the substrate is made on the platform to which the die is bonded, then R_S will be given by the spreading resistance through the substrate to the back surface. If the ground contact is made on the top surface of the chip, R_S will be the resistance through the substrate to the nearest ground contact. The substrate resistivity for bipolar LSI circuits usually ranges from 1 Ω cm to 20 Ω cm. To illustrate a typical value of R_S consider an NPN transistor with a buried layer 15 μm x 30 μm on a 3 Ω cm substrate 10 mil thick. For the case where the current path is long compared to the radius of the contact area the spreading resistance is given by $\rho/2a$ where ρ is the resistivity in Ω cm and a is the diameter in cm of the circular contact area. For a diffused region $a = (3X_jW_1W_2/4\pi)^{1/3}$ where X_j is the diffusion depth and W_1 and W_2 are the dimensions of the rectangular area. For

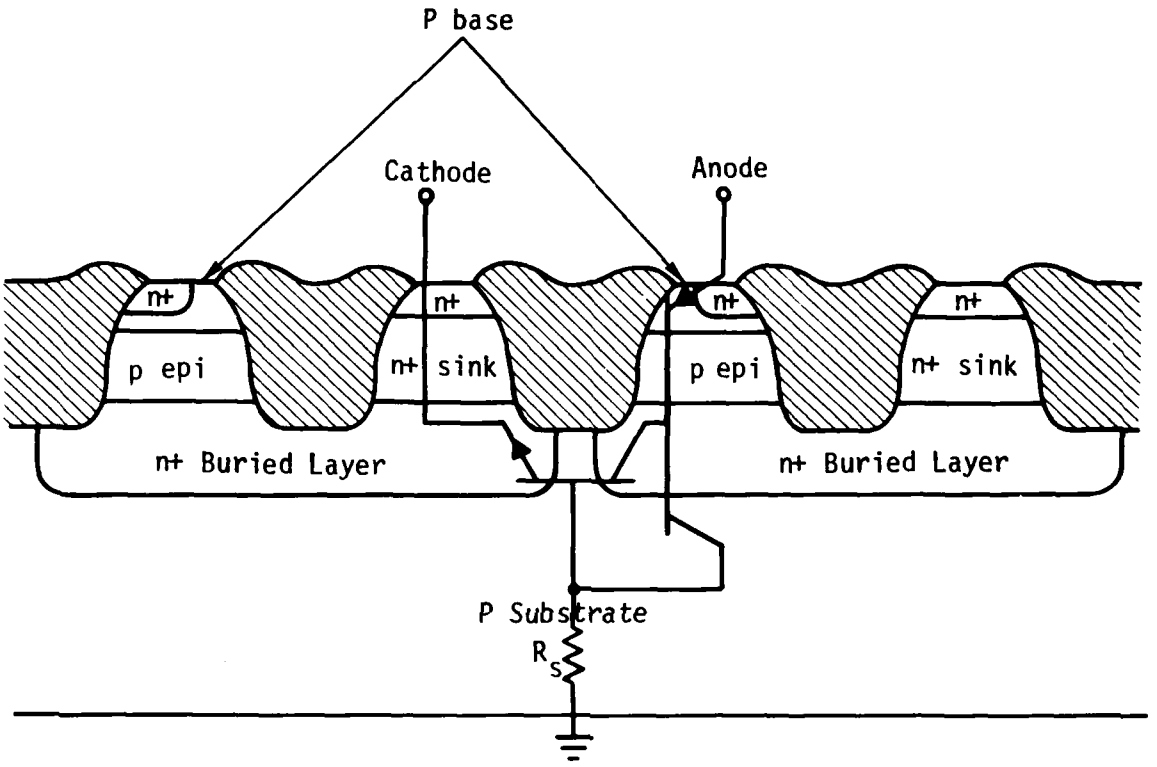


Figure 4. Cross section of two closely spaced isoplanar NPN transistors showing substrate latchup path.

this example R_S = 2.2 KΩ if the ground contact is made to the top surface and the die attach is non-conductive. A current of 350 μA through this resistance would maintain J3 in forward bias.

However, for most bipolar LSI devices, the die attach is conductive. This may lower the value of R_S since the back surface is an equipotential and the current path is altered.

In order to investigate the possibility of substrate latchup on the 9408, two closely spaced NPN transistors in the output circuit were isolated from the rest of the circuit on one unit. The parasitic NPN and PNP transistor gains were measured as a function of current. The peak NPN gain was .55 which occurred at ~1mA. The vertical PNP gain reached a maximum of .1 between 10 mA and 100 mA. Thus the product gain at all current levels was well below 1. As expected the path could not be latched when positive voltage was applied from anode to cathode with the gates open.

4.3 93471

The 93471 is an isoplanar 4096X1 static RAM which uses an ECL memory cell. The T^2L to ECL buffers, peripheral circuitry and I/O are all Schottky T^2L. As with the 9408 the chip was photographed, the interlevel dielectric removed and the chip rephotographed to reveal the first level metal and individual components. The first region analyzed was the ECL memory cell. Each isolated region in the memory cell contained a diffused resistor and a multiple emitter transistor. An angle lap and stain of the memory cell indicated that the parts were made with a p epitaxial layer. Discussions with Fairchild revealed that while parts can be made with either n or p epi, p epi is preferred because of the better control of the NPN current gain. All of the parts that were investigated in this study were made with p epi. For the p epi process there are no parasitic PNPN paths within the same isolation region in the ECL memory cell. A detailed

investigation of the peripheral and I/O circuitry revealed that all components were isolated from one another by oxide sidewalls. Therefore on the 93471 device the only parasitic PNPN path involved the substrate. The chip was surveyed to find the closest spaced components in the peripheral and I/O circuitry. Two pairs of closely spaced NPN transistors were selected and isolated from the rest of the circuitry. As with the 9408 the vertical PNP and lateral NPN parasitic transistors were probed to determine the gain vs. current values. The maximum NPN gain was .62 and occurred between 1 and 2 mA. The maximum vertical PNP gain was .22 and was fairly constant between 10 μA and 10 mA. Thus the product gain was less than one over the whole current range. As expected latchup was not observed.

4.4 AD571

The AD571 is a monolithic 10 bit A/D converter which uses I^2L for the internal clock and successive approximation registers. It also uses laser trimmed thin film resistors for the R-2R ladder, a buried zener reference diode, linear circuits, MOS capacitors, and tri-state T^2L output buffers. The basic process is junction-isolated linear which uses double diffused transistors in a relatively thick n epitaxial layer on a p substrate. Thus the I^2L gates use a low performance first generation double-diffused structure. A complete process and circuit description of the device along with a circuit schematic has been published.[12] A composite photomicrograph was made of the chip at 125X. Since the part uses single level metal only one photograph was necessary. The photomicrograph was checked against the circuit schematic to verify the schematic and identify each component. The first step in the identification of parasitic PNPN paths was to locate isolation regions containing multiple components. Excluding the I^2L circuitry which was all contained within a single isolation region, 15 regions were found which contain multiple components. These 15 regions were identified on the circuit schematic in order to perform a preliminary analysis and eliminate those PNPN paths which were

obviously latchup free. Five of these regions were eliminated because they a) contained only a Darlington transistor pair, b) contained only lateral PNP transistors or c) had the anode and cathode connected by metal. This left 10 regions containing multiple components which might be latchup susceptible. Since three of these regions contained 5 or more transistors, the total number of distinct PNPN paths was quite large. Once the potentially latchable paths are identified, one can proceed either by performing a detailed circuit analysis or electrical characterization of the paths. In this study the characterization was performed after the preliminary circuit analysis. All of the PNPN paths within the 10 susceptible regions were decoupled from the circuit. This decoupling was performed by Naval Weapons Support Center (NWSC) Crane by scratching the glassivation over the metal line and etching the metal lines. Each of the PNPN paths was probed and characterized on a curve tracer to determine if it would latch with the gates open. If it latched, the holding current and holding voltage were recorded. Every path tested could be latched. The holding currents ranged from less than a microamp to 1.6 mA.

The next step was to perform a detailed circuit analysis to determine if the D.C. bias conditions were proper for latchup. This analysis was performed both by hand and with the aid of the SPICE circuit analysis code.[8] Each path was analyzed using the worst case bias conditions allowed by the specification. The path was eliminated if it could be shown that the anode was always negative with respect to the cathode or that J1 or J3 was always reversed biased. In addition, it was discovered that several of the parasitic PNPN paths were being utilized in the circuit as SCRs in the "on" state but that the current to the path was intentionally limited. The results of the circuit analysis indicated that while many of the paths could be eliminated there still remained paths in seven different isolation regions that could not be eliminated. These paths were discussed with Mr. Paul Brokaw of Analog Devices who was instrumental in the design and development of the circuit. With his assistance in analyzing the remaining

paths the number of potentially latchable paths was reduced to one path which is illustrated in Figure 5. This path is located in the Bipolar Offset circuit which controls whether the output bits read on a scale of 0 - 10V or -5 to +5V. The bipolar offset circuit was modeled on SPICE as shown in Figure 5. The function of this circuit when it is in operation (Bipolar offset pin open) is to inject a positive current into the comparison node (node 4) equal to half the full scale current. Q360 and Q361 make up a differential amplifier which is disabled when the bipolar offset pin is grounded. The parasitic PNPN path is shown by the the coupled transistors Q358A and Q360. This path in the actual device runs from the emitter of Q358 (a lateral PNP transistor) to the epitaxial layer through the base and emitter of the NPN transistor Q360. The worst case bias conditions for latchup are with the bipolar offset pin grounded (as shown in the Figure) and V+ at a maximum. V_{IN} is the analog input, VAC the a.c. common node and node 4 the input to the comparator. The comparator is shown as a 100 KΩ load to ground. The photocurrent generators (F1 - F17) are scaled to the collection volume of each junction and controlled by the current loop R6,VA. To investigate the latchup characteristics of the circuit SPICE runs were made both with a voltage pulse on VAC to simulate electrical induced latchup and with a pulse on VA to represent photocurrent induced latchup. The results are shown in Figure 6. In 6-a the voltage on the analog common node was pulsed from .2V (nominal bias) to 1.0V (maximum rating for node). VAC connects to the cathode-gate of the parasitic SCR through a 20 KΩ resistor. When VAC is pulsed to 1V the anode of the parasitic SCR drops to a voltage of .98V and stays there after the pulse is removed. The anode current is 4.5 mA in the "on" state. When this occurs, the voltage at node 4, the input to the comparator is pinned at .92V. This would cause all bits to read the same regardless of VIN. The result of pulsing the photocurrent generators is shown in Figure 6-b. With a voltage of 1V on VA the loop current is 1 μA. This is the minimum photocurrent which was set for the smallest junctions. Other photocurrents were scaled according to area. The large substrate photocurrent, F14 was 2.1×10^4

BIPOLAR OFFSET CIRCUIT

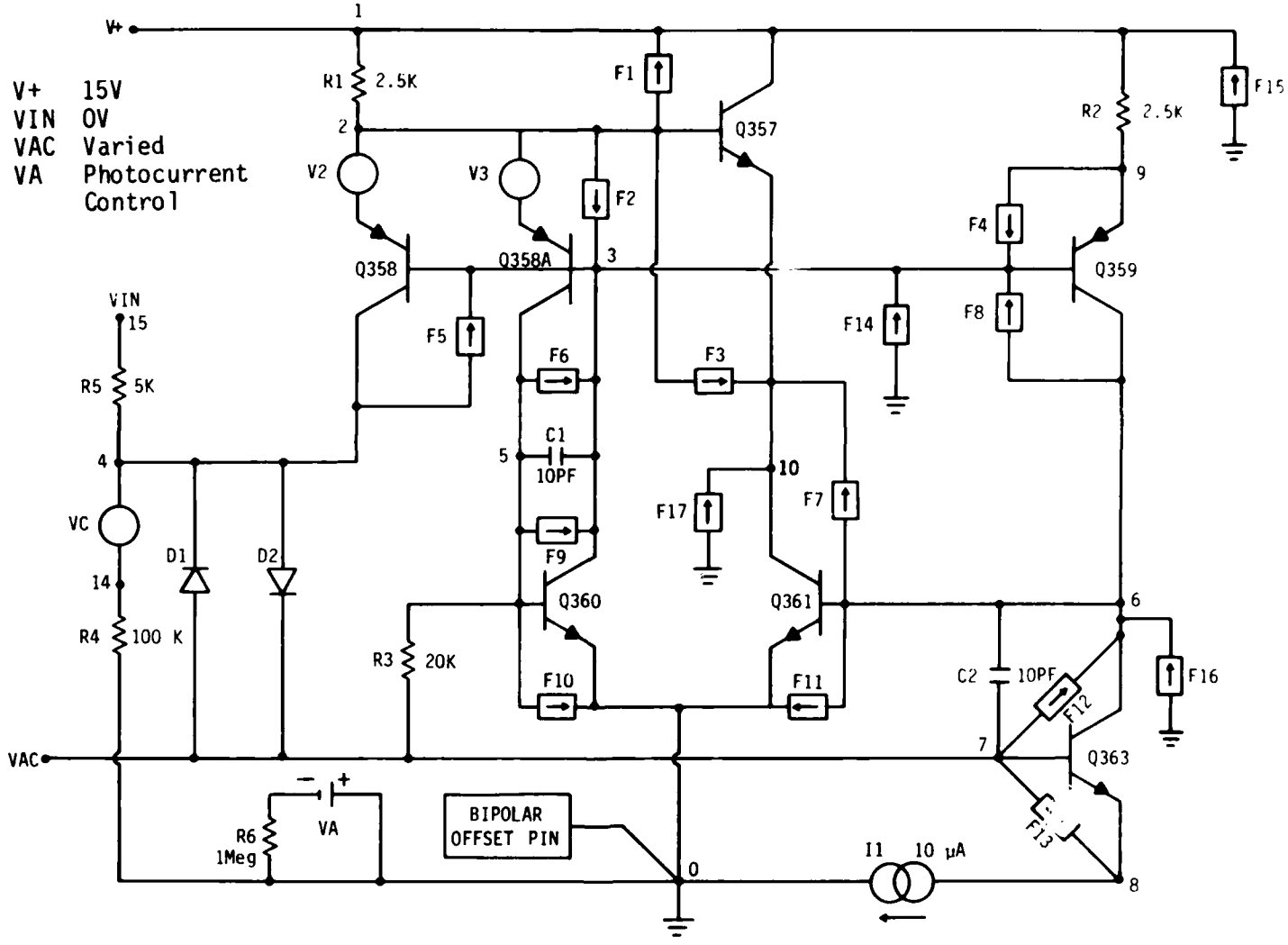
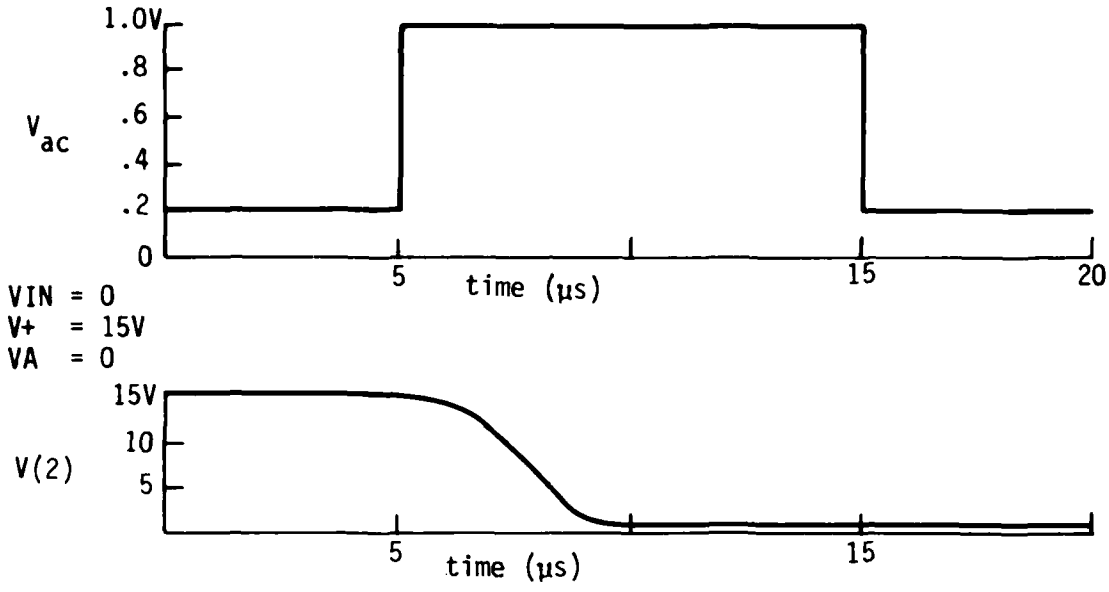
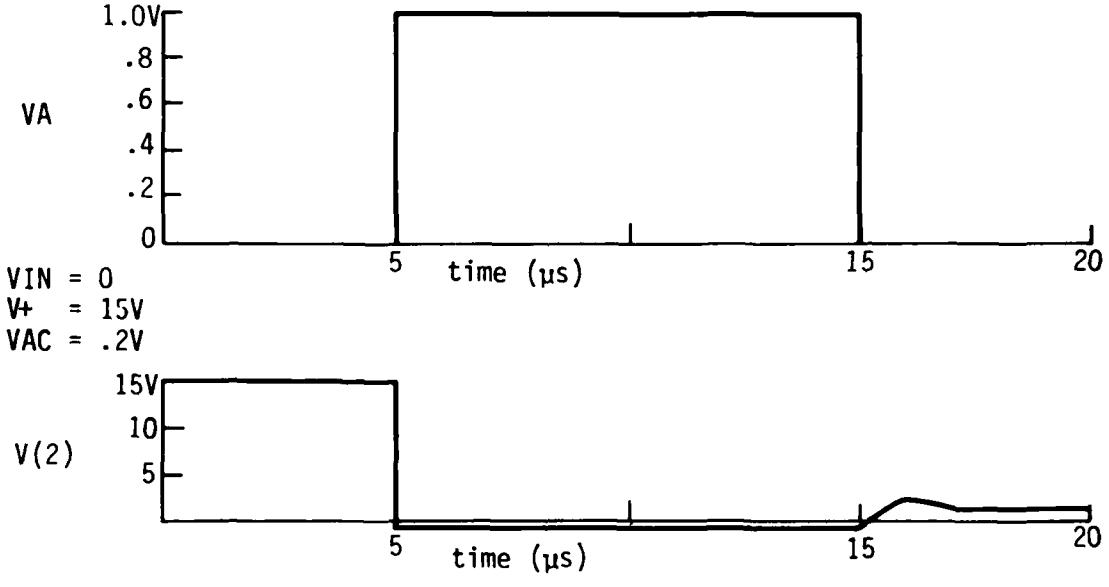


Figure 5. AD571 bipolar offset current circuit with parasitic PNPN path and photocurrent generators.



a.) Electrical induced latchup in bipolar offset circuit. Node 2 is the anode of the parasitic PNPN path.



b.) Photocurrent induced latchup in bipolar offset circuit. Node (2) is the anode of the parasitic PNPN path.

Figure 6. Voltage waveforms showing electrical and photocurrent induced latchup in AD571 bipolar offset circuit using SPICE.

times this baseline value and during the VA pulse it pulled the anode negative. When the photocurrent pulse is removed, the anode voltage goes to the "on" state value of .98V and again node 4 is pinned at .92V. Again the anode current went to 4.5 mA.

These simulated SPICE runs indicate that the bipolar offset circuit will latch and cause all bits to read the same independent of VIN. The parasitic PNPN path from emitter Q358 to emitter Q360 was experimentally determined to latch when detached from the circuit. It has a holding current of 1.5 mA which is below the current available to the path as determined by the SPICE runs (4.5 mA). Based on these results, the bipolar offset circuit should latch when the VAC line is electrically pulsed to a value of 1V. An electrically induced latchup test was conducted on 5 units to verify these results. The circuits were operated with V+ = 15V, VIN = 10V and 0V and the bipolar offset pin grounded. B&C was first held at V+ then grounded and DR was observed to go low indicating the data was ready to be read. All bits were verified for proper data. VAC was then pulsed to 1V and returned to .2V. No change was observed in the bits for either VIN condition. These results indicate that no latchup occurred. The radiation induced latchup tests (discussed in a later section) also failed to produce a latch in this circuit. Although the analysis, circuit simulation and characterization of the latchup path indicate that latchup should occur, neither the electrical induced or radiation induced tests were successful in causing latchup.

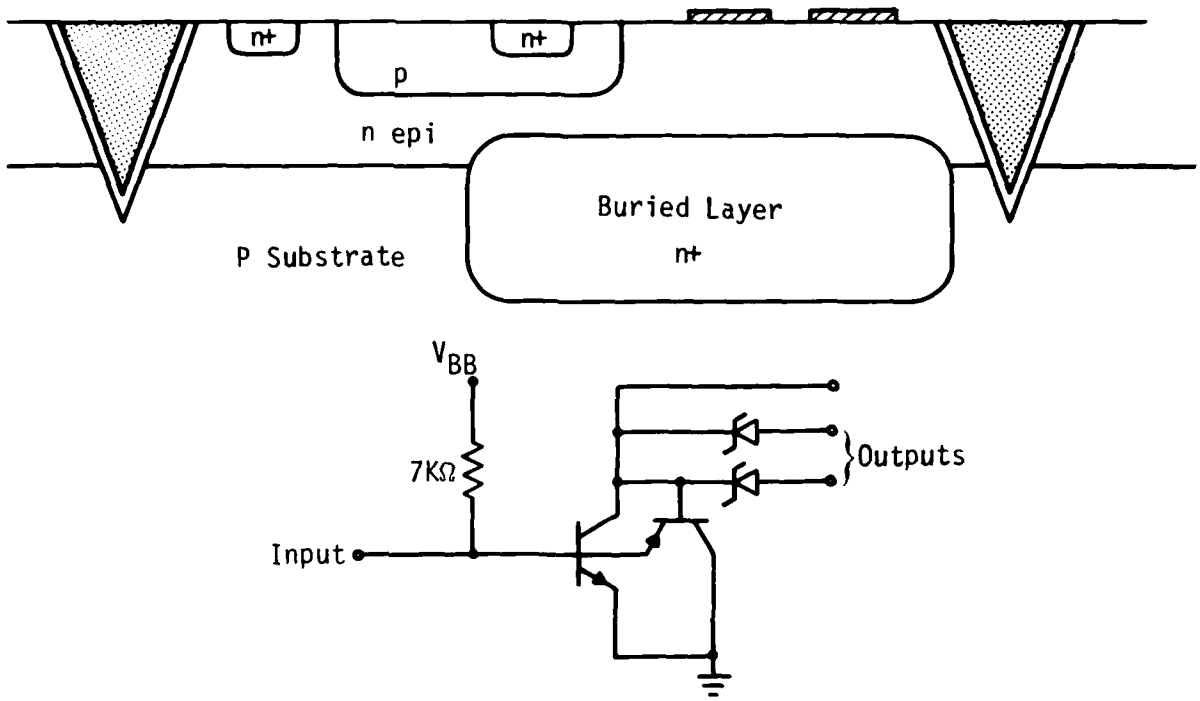
In addition to the analysis of the PNPN paths within isolation regions, a study was also made of type 1 substrate latchup. Several parasitic vertical PNP and lateral NPN (buried layer-substrate-buried layer) transistors were characterized for gain vs current. The maximum PNP gains ranged from 2 to 6 and the NPN gain on closely spaced adjacent components was ~.3. On several substrate PNPN paths which were decoupled from the circuit, latchup could easily be induced under worst case conditions with

the gates open. However, when either the back side of the chip or the V- contact was grounded the latch was broken. A variable series resistor was added to the substrate (cathode-gate) lead to determine its effect on the holding current. With a 1 KΩ resistor in series with R_S (the parasitic substrate shunt resistance) the holding current was typically 1-2 mA. As expected, the holding current increased nearly linearly as the resistance was lowered. With only the resistance R_S present the holding current was greater than 300-500 mA at which point the PNPN path sustained permanent damage. The conclusion is that for the AD571 the value of R_S is sufficiently low that substrate latchup will not be a problem.

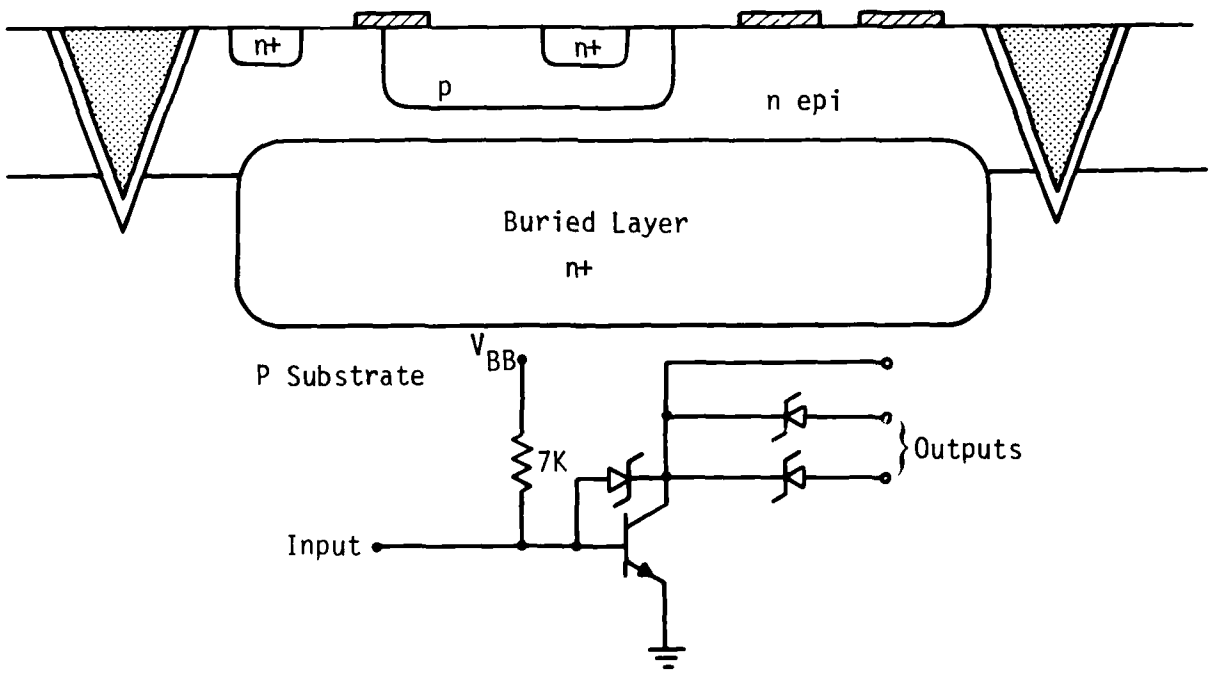
4.5 ISL/STL

Integrated Schottky Logic (ISL) and Schottky Transistor Logic (STL) are two forms of high density bipolar logic similar to I^2L. Both ISL and STL use single input multiple output inverters as the basic logic unit. However, they differ from I^2L in as much as the NPN switch is operated in the normal (noninverted) mode and current is supplied to the gate by a voltage supply (V_{BB}) and a resistor. In ISL the NPN switch is kept out of deep saturation by a vertical parasitic PNP transistor and in STL by a collector-base Schottky clamp. The isolated outputs are Schottky contacts to the NPN collector region. A two output inverter in ISL is shown in Figure 7 for the Harris polyplanar process.

At the present time Harris Semiconductor is developing a 1580 gate array that will be offered in either ISL or STL. This array will be junction-isolated with oxide sidewalls using the polyplanar process. The input and output buffers will be Schottky T^2L. The latchup analysis of this array did not follow the analysis of other bipolar LSI circuits since fully functional arrays were not available in both ISL and STL versions. Therefore the analysis was separated into two parts. The I/O buffers were analyzed by studying the mask set and the internal ISL/STL inverters were analyzed by studying a special test chip.



a.) Cross section and circuit diagram of Harris two output ISL inverter.



b.) Cross section and circuit diagram of Harris two output STL inverter.

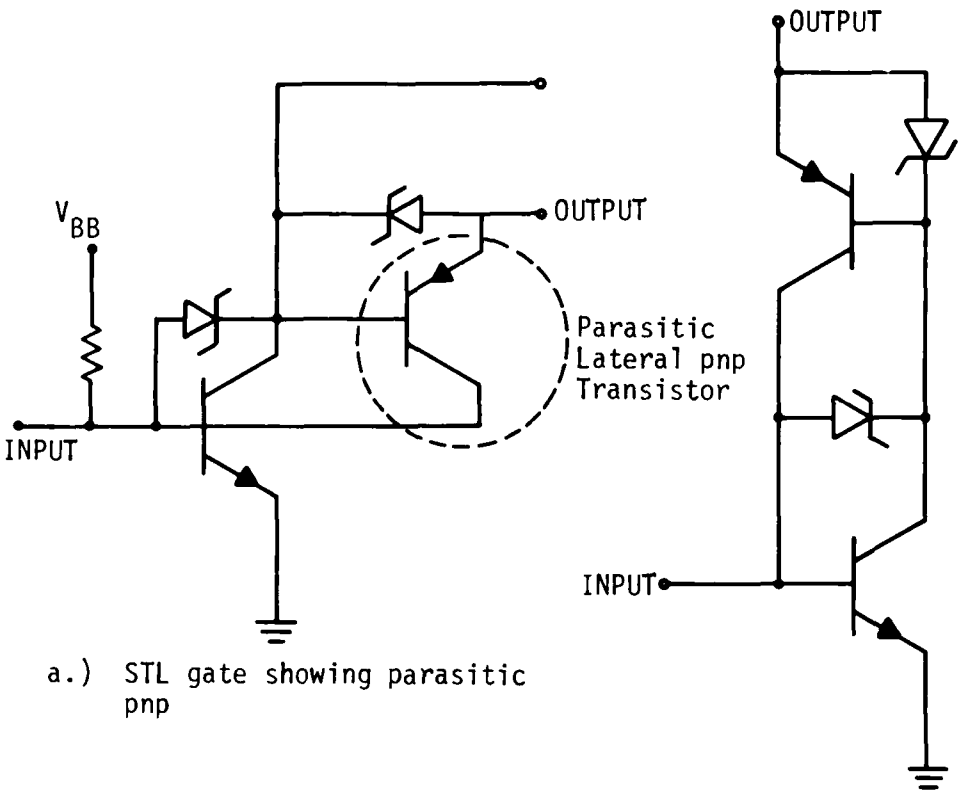
Figure 7. Cross section and circuit diagrams of Harris ISL and STL inverters.

The identification of parasitic PNPN paths with isolation regions in the I/O buffers was accomplished by studying a mask set obtained from the manufacturer. The result of this study was the conclusion that all components are isolated by oxide-sidewalls. Therefore, the only parasitic PNPN paths in the I/O involve the substrate.

Within the ISL/STL logic array the only parasitic PNPN path is from the Schottky collector (output) through the epitaxial layer, the p type NPN base region and the NPN emitter. Such a path exists since the Schottky contact can function as a p type region injecting minority carriers at high current density.[13] A similar path has been shown to cause latchup in Schottky T^2L logic circuits.[14] The characteristics of this type of latchup path have been studied in detail and a model developed to predict the maximum gain of the parasitic lateral PNP transistor.[15]

However, an analysis of this parasitic PNPN path within the context of the ISL/STL inverter shows that the path is an integral part of the circuit. This is illustrated in Figure 8 for an STL inverter. Since the inverter input node is the cathode-gate of the parasitic SCR, a positive voltage pulse on this node will latch the SCR and the output will remain in the "on" state until power is removed. Thus if this path could be latched, the inverter output would always be low and the circuit would not function properly. Proper electrical operation of the circuit guarantees that the path does not latch. Since the parasitic PNP gain is higher at elevated temperature a useful latchup screen for this circuit would be an operational elevated temperature test.

The results of the latchup analysis on the Harris ISL/STL gate array are that if the circuit is operational under elevated temperature, the only potential latchup path is one between closely space components involving the substrate.



a.) STL gate showing parasitic pnp

b.) Redrawn circuit configuration showing parasitic SCR

Figure 8. Circuit configuration of parasitic PNPN path in STL inverter.

Although no closely spaced buffer components were available on the test chip, parasitic gains were measured within the ISL and STL gate structures. The vertical PNP gain was measured for the full buried layer STL gates (similar to I/O structures). For non gold-doped chips the maximum gain was .70 and for chips which were gold-doped the gain was .14. A lateral NPN parasitic transistor from the buried layer of one gate to the buried layer of an adjacent gate was also characterized. The maximum gain for the non gold doped circuits was .14 and for the gold-doped, .014. The spacing between these gates (base width) was 40 μm. The minimum spacing between adjacent components in a buffer is 10 μm. Predications of worst case parasitic gains based on minimum spacing are discussed in Section 5.

5. RESULTS OF ANALYTICAL CHARACTERIZATION

In section 3.2.2 a general description was given for the various modeling approaches that were investigated in this study to perform the characterization of the PNPN paths. In this section the results of that study are presented.

5.1 1-D CLOSED FORM β APPROXIMATIONS

In many cases the product gains are either much greater than one or much less than one. If the product gain is much greater than one and there is no effective way to reduce the product gain without severely compromising the electrical performance of the overall circuit, then the latchup analysis for the path becomes a circuit analysis to determine the worst case bias conditions for the path. This is the case for the PNPN paths within isolation regions on the AD 571. It is probably the case for all junction isolated linear circuits. Trying to reduce parasitic gains to limit $\beta_n \cdot \beta_p$ would assure that the intended transistors would not have sufficient gain to work in the circuit.

For the case where the parasitic gain product is much less than one, the only modeling necessary is to assure that no major changes occur in the process such that the gain product approaches one. Simple first order approximations can be used to identify the major variables that control gain. Once these are known, the expressions for gain can be used to indicate the limits of change allowed in these variables before latchup becomes a potential problem. In this case a worst case approximation for maximum gain is probably sufficient.

For a vertical parasitic transistor with a uniformly doped base region the following expression can be used:

$$\beta(MAX) = \frac{1}{\left[\cosh\left(\frac{W}{L_B}\right) + \frac{N_B D_E L_B}{N_E D_B L_E} \sinh\left(\frac{W}{L_B}\right)\right] - 1} \qquad (1)$$

This relation includes both the base transport factor (cosh term) and the emitter efficiency (sinh term). In this expression W is the base width, L_B and L_E the minority carrier diffusion length ($\sqrt{D\tau}$) in the base and emitter respectively, N_B and N_E the base and emitter doping levels and D_B and D_E the base and emitter minority carrier diffusion coefficients.

If the vertical parasitic transistor has a graded doping profile in the base region, then the first order approximation for maximum gain is:

$$\beta(MAX) = \frac{1}{\left\{\cosh\left(\frac{W}{2\,L_B}\right)\left[1 + \frac{D_E N_B^*}{D_B N_E L_E}\right]\right\} - 1} \qquad (2)$$

In this expression the product $N_B\ L_B$ has been replaced by the Gummel number N_B which is the integral of the base doping over the base width.

$$N_B^* = \int_0^W N_B(x)\, dx$$

Again the first term in the brackets is the base transport term and the second term the emitter efficiency. In these expressions for the uniform and nonuniform base gain predictions the emitter-base space charge recombination term and the surface recombination term have been assumed to be negligible.

A considerable amount of modeling has been performed on lateral PNP transistors, such as those used in linear integrated circuits. However, as noted by Estreich[6], little attention has been paid to lateral parasitic, low gain transistors such as those that often appear in parasitic PNPN paths. In Estreich's analytical treatment of parasitic lateral transistors, an expression is derived for gain with an externally applied electric field in the base region. For the case where this field is zero, the first order approximation (base transport term only) for β is as follows:

$$\beta(MAX) = \frac{1}{\cosh\left(\frac{W}{L_B}\right) - 1 + \frac{A_V}{A_L} \sinh\left(\frac{W}{L_B}\right)} \qquad (3)$$

where A_V is the area of the emitter injecting current vertically and A_L is the emitter area injecting current laterally. This is illustrated in Figure 9 in which a lateral NPN transistor between two buried layers for the Fairchild Isoplanar process is shown. The term which accounts for the emitter current loss vertically can significantly reduce the predicted β if the ratio A_V/A_L is large.

By using the above three equations for calculating the maximum parasitic gains of the transistors, one can get a reasonable worst case approximation for the β product. As expected, the major parameters controlling the gain are base width and minority carrier diffusion length in

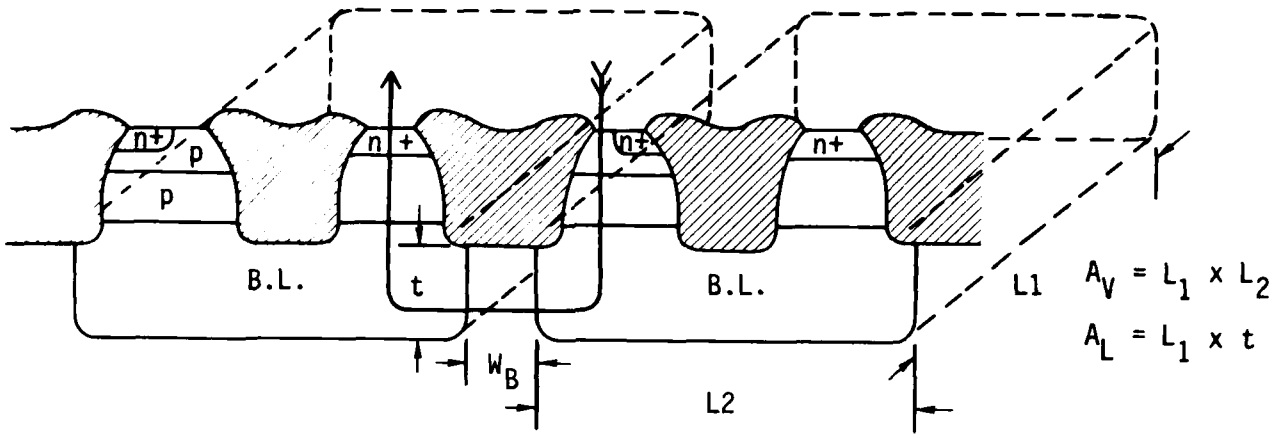


Figure 9. PNPN path in Isoplanar process showing lateral substrate NPN transistor between two buried layers.

the base, L_B. Since L_B depends on lifetime, a reasonable approximation of the lifetime is very important. Substrate lifetimes in good, low impurity, low defect density material are usually between one and ten microseconds. However, high temperature processing can introduce unwanted impurities and large crystal defect densities which can significantly degrade lifetime. Lifetimes in epitaxial material have not been well characterized, but lifetimes in heavily doped material ($>10^{17}$ cm^{-3}) are known to decrease nearly linearly with doping density.[16] Gold doping is also known to significantly reduce lifetimes and curves have been established to define the lifetimes as a function of gold concentration. For a worst case analysis for non gold-doped silicon, a maximum lifetime of 2 to 10 μs can be assumed for the lightly doped regions and for heavily doped regions the lifetime can be degraded according to the following relation.[16]

$$\tau(n) = \frac{\tau_o}{1 + \frac{N}{5 \times 10^{16}}} \qquad (4)$$

If the emitter doping level is comparable to or lower than the base doping, then the emitter efficiency term may be the dominant term. In this case N_E and N_B (or N_B^*) will significantly influence the gain as well as D_E, D_B and L_E. If one of the parasitic transistors is a lateral device, as illustrated in Figure 9, then A_V and A_L will be important parameters.

Using the first order approximations given in equations 1-3, one can establish design rules to assure that the parasitic gain product remains below one with whatever safety margin one wishes to impose.

As an example of the application of equation 3 for lateral NPN gain two sets of parametric design curves are derived. In Figure 10 the maximum current gain β is plotted against W/L_B for various values of A_V/A_L. Increasing either W/L_B or A_V/A_L significantly reduces β. A_V/A_L can be increased by increasing the area of the buried layers under components or decreasing the length of the buried layer edge adjacent to another buried layer. W/L_B can be increased by increasing the minimum spacing between buried layers or decreasing substrate lifetime. Figure 11 is a plot of the ratio W/L_B vs. lifetime for various base widths and substrate resistivities. This graph can be used by selecting from Figure 10 the desired β for the A_V/A_L ratio. An example is given for a $\beta < 1$ with a ratio $A_V/A_L = 5$. This gives a value of $W/L_B = .2$ or greater. Therefore, any combination of lifetimes, substrate resistivities and buried layer separations (W) lying above the line $W/L_B = .2$ will produce the desired results, i.e. $\beta_{NPN} < 1$. As an example, if the substrate resistivity is 3 Ω cm and the substrate lifetime is 1 μSec, then the buried layers will have to be separated by a value slightly greater than 10 μm.

A comparison of the gain prediction equation to actual measurements on an LSI device was performed for the large adjacent transistor pair on the 93471. The maximum gain of the parasitic NPN was .56, the A_V/A_L ratio was 18, the substrate resistivity 3 Ω cm and the separation of buried layers of ~8 μm. From Figure 10, W/L_B is ~1. From Figure 11 the lifetime is between 2 and 3 μs which is a reasonable number for substrate lifetime.

Another example of the use of this simple relation for β_{NPN} is shown in Table III for the Harris STL technology. As discussed in Section 4.5, the gain of the vertical parasitic PNP was .70 for non gold-doped and .14

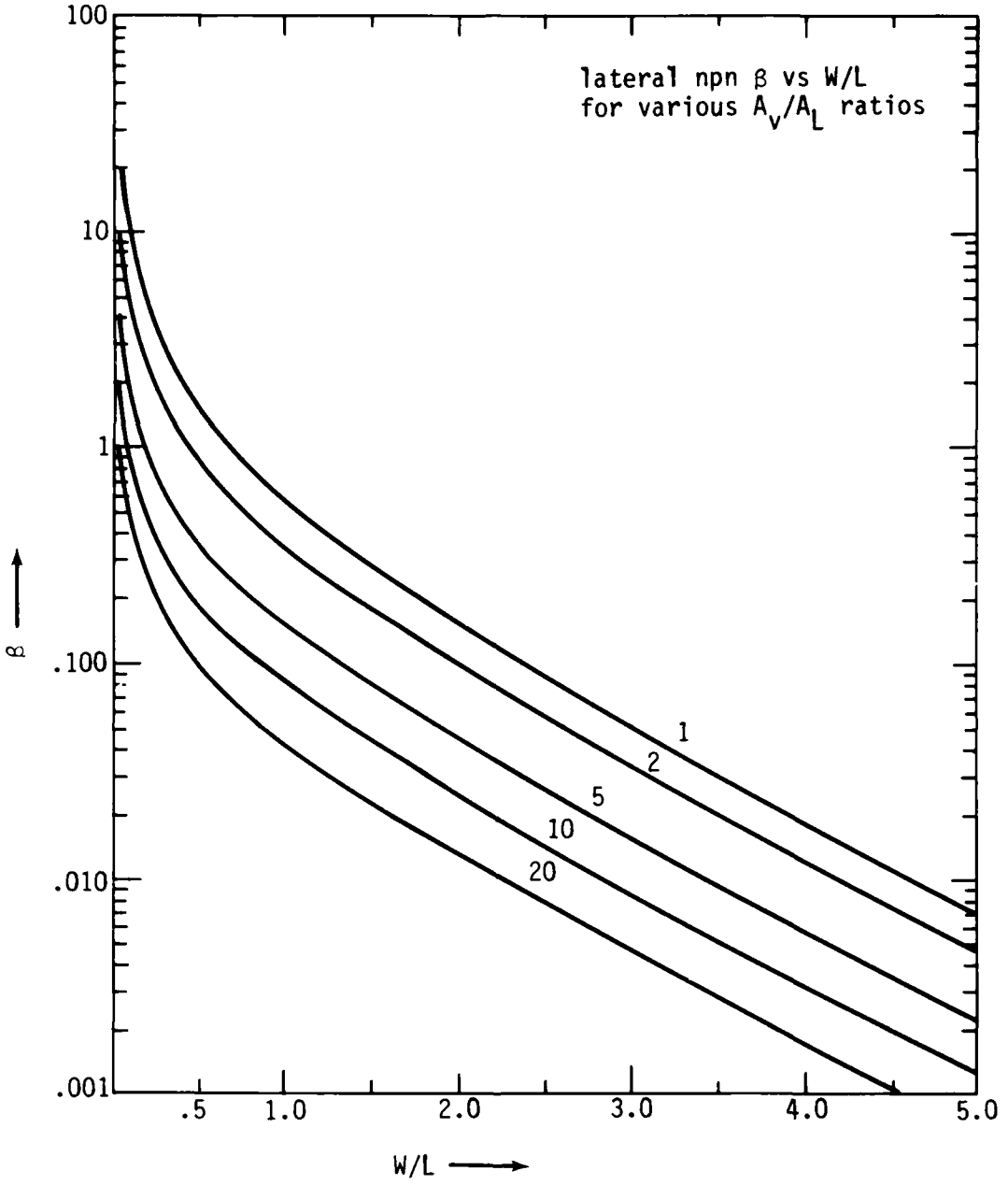


Figure 10. The current gain of a lateral substrate npn transistor (β) vs W/L_B for various A_V/A_L ratios.

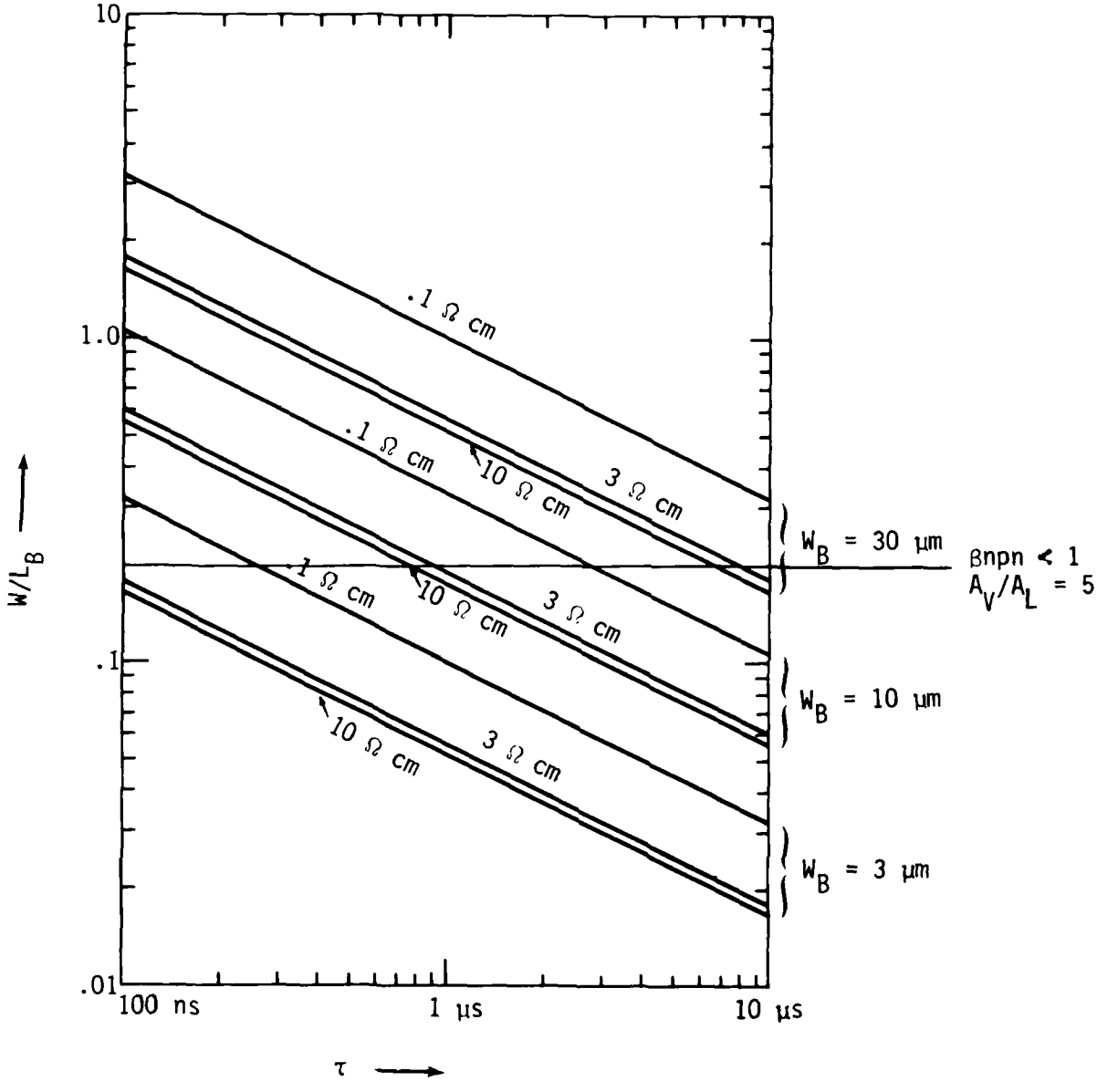


Figure 11. The ratio of W/L_B of a lateral substrate NPN transistor vs lifetime for various base widths and substrate resistivities.

TABLE II. Calculated NPN gains versus W_B and A_V/A_L.

Non gold-doped τ = 2.15 μS, L_B = 68 μm

A_V/A_L	W_B = 10 μm	W_B = 5 μm
10	.67	1.35
5	1.33	[2.69]
2	[3.27]	[6.67]

Gold-doped τ = 118 nS, L_B = 16.3 μm

A_V/A_L	W_B = 10μm	W_B = 5 μm
10	.149	.316
5	.289	.622
2	.667	1.49

[ ] indicates $\beta_n \cdot \beta_p > 1$

for gold-doped devices. From the results of the measured parasitic NPN gain for a 40 μm base width the substrate lifetimes were calculated to be 2.15 μs for the non gold-doped device and 118 ns for the gold-doped device. In Table III, calculated NPN gains are given for various A_V/A_L ratios and W_B values for both non gold-doped and gold-doped devices. The gain values contained within boxes are those for which the product of NPN and PNP gains exceeds one. Even for an A_V,A_L ratio of 2 and a 5 μm spacing of components, the gain product is less than one for the gold-doped devices. Therefore, it appears that for the Harris ISL/STL gates gold doping will assure the prevention of substrate latchup.

Although the gain formula for lateral substrate NPN transistors given here is only a first order approximation, it gives results which are good enough to establish basic guidelines for latchup free circuits.

5.2 1-D CODE CALCULATIONS OF β

If the parasitic β product for a specific PNPN path is close to one, then a more detailed analysis is required in order to predict whether or not the path is potentially latchup susceptible for a specific layout and process. The more detailed approach is also necessary to determine design rules, both layout and processing, required to assure that the path will not latch or to limit the holding current to a value greater than the current available to the path. A current dependent gain can be approximated using a 1-d semiconductor device physics code which solves the Poisson and continuity equations using numerical analysis techniques. The code used in this study is the transient analysis PN code. Inputs to the code are position dependent doping densities, position dependent lifetimes and doping density dependent mobilities. The DC current gain vs base-emitter voltage (V_{BE}) can be calculated by stepping V_{BE} to fixed values and maintaining the VBE until an equilibrium solution for I_C and I_B has been reached. Also by plotting I_C and I_B vs V_{BE} all of the DC model input

parameters for the Gummel-Poon bipolar transistor model, such as that used in SPICE, can be obtained.

The advantage of using the code to calculate gain is that a complete β vs I_E curve can be generated for each parasitic transistor. This allows for the calculation of $\beta_N \cdot \beta_p$ vs I_{anode} which can be used to determine the holding current ($\beta_N \cdot \beta_p = 1$) and the maximum gain product. In the approach discussed in the previous section only the maximum gains are calculated. If these maximum gains occurred at different emitter currents then the product $\beta_n(MAX) \cdot \beta_p(MAX)$ will be an overestimate of the maximum possible gain product.

The disadvantage of using this approach is that two dimensional effects, such as vertical injection in the lateral parasitic transistor, are not taken into account. As will be seen in the next section, such 2-d effects can be modeled by using a circuit code in which a parasitic diode is included.

The true test of the code calculations is their ability to predict parasitic gains equal to the "effective" gain of the parasitic transistor in the actual PNPN structure. The problem of demonstrating the effectiveness of the code is twofold: 1.) Access to test devices (parasitic transistors) with the proper lead arrangements to measure "effective" gains and 2.) knowledge of the geometry, doping profile and lifetimes of test devices so that they can be accurately input to the code. Unfortunately neither criteria, 1.) or 2.) could be fulfilled with any of the LSI devices which were analyzed for latchup in this study. Therefore, a specially designed and characterized test structure built for a CMOS latchup study at Sandia Laboratories was obtained. This test chip known as LURIC (Latch-Up and Radiation Integrated Circuit) contains a series of Latch-Up Structures (LATUS) used to characterize the latchup susceptibility of CMOS latchup paths as a function of top surface geometry and parasitic resistances.

Figure 12 is a mask overlay of subchip A6 on the LURIC test chip which contains four of the LATUS test devices. In structures 35 and 36 of this subchip and structures 29 and 30 of subchip A5, the lateral PNP transistor base width is varied from 10 μm to 40 μm while maintaining all other parameters constant. The four layer latchup path is from a p+ diffusion (p channel source or drain) through the substrate (n type) the p well and out through an n+ diffusion in the p well (n channel source or drain). In test chip A6, the spacing between the p+ and p well is varied. This value is the base width of the lateral PNP. The LATUS test structures were chosen to verify the PN code model calculations since they included a complete four layer path along with terminal (probe pad) access to each of the regions of the parasitic vertical NPN and lateral PNP transistors.

Four wafers of LURIC test chips were obtained, two gold-doped and two non gold-doped. One non gold-doped wafer was sectioned and sent to Solecon Labs for profiling using spreading resistance measurements. The results of the vertical NPN profile are given in Figure 13 and the p+ into n substrate profile given in Figure 14.

The doping density profile for the vertical NPN transistor, shown in Figure 13, was divided into 30 mesh regions and input to the PN code. Several runs of this profile were made with varying minority carrier lifetime in the base region (P well) and a collector (substrate) lifetime of 1 μs. The base-emitter voltage was varied between .5 and 1.0 V to produce collector currents in the range of interest and the collector-emitter voltage was set at 5 V. The energy level for the single level SRH recombination model was set at mid-gap which maximizes the recombination rate. Mobility versus doping density values were obtained from standard texts. The cross sectional area was obtained from a photomicrograph of the n+ diffused region and 2 μm was added to each side for lateral diffusion. The cross sectional area thus calculated was 9.15×10^{-5} cm^2.

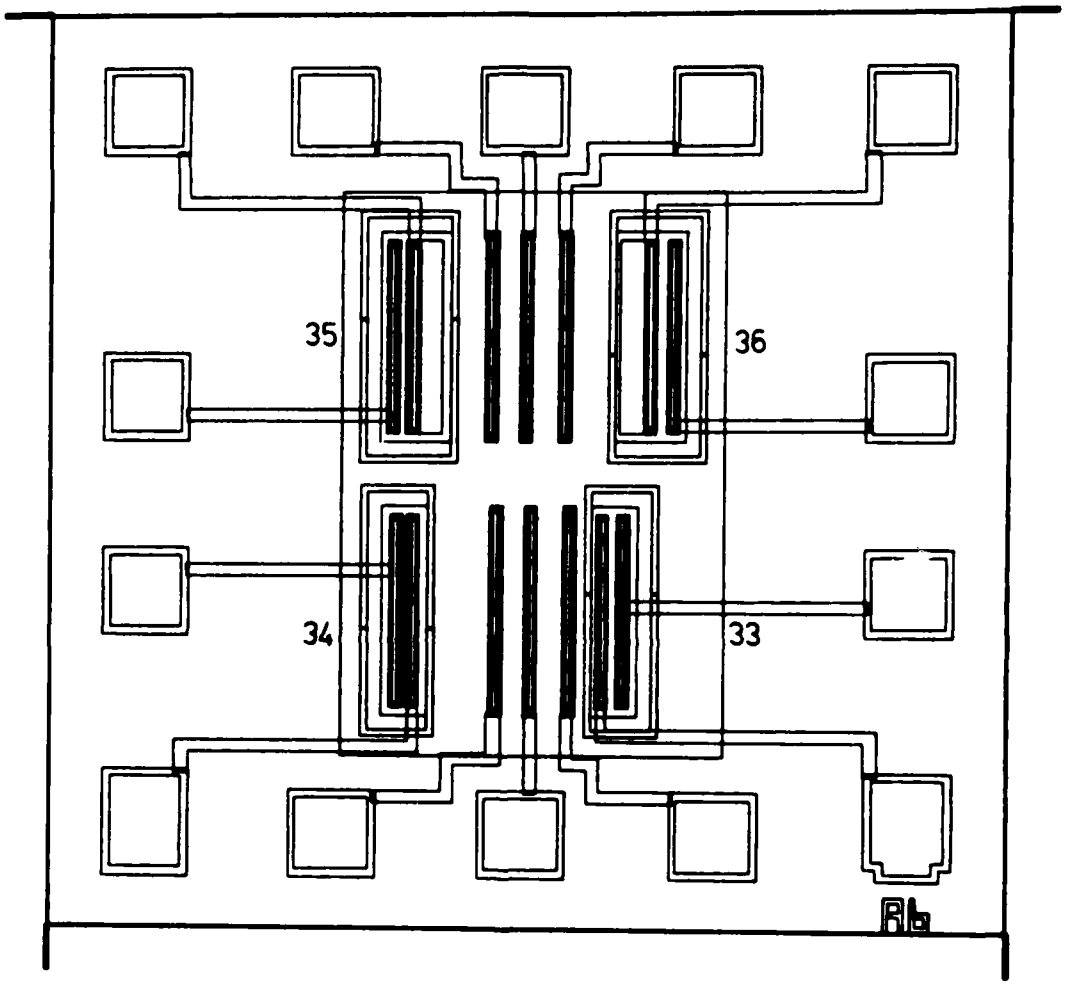


Figure 12. Four latchup test structures on Sandia LURIC test chip.

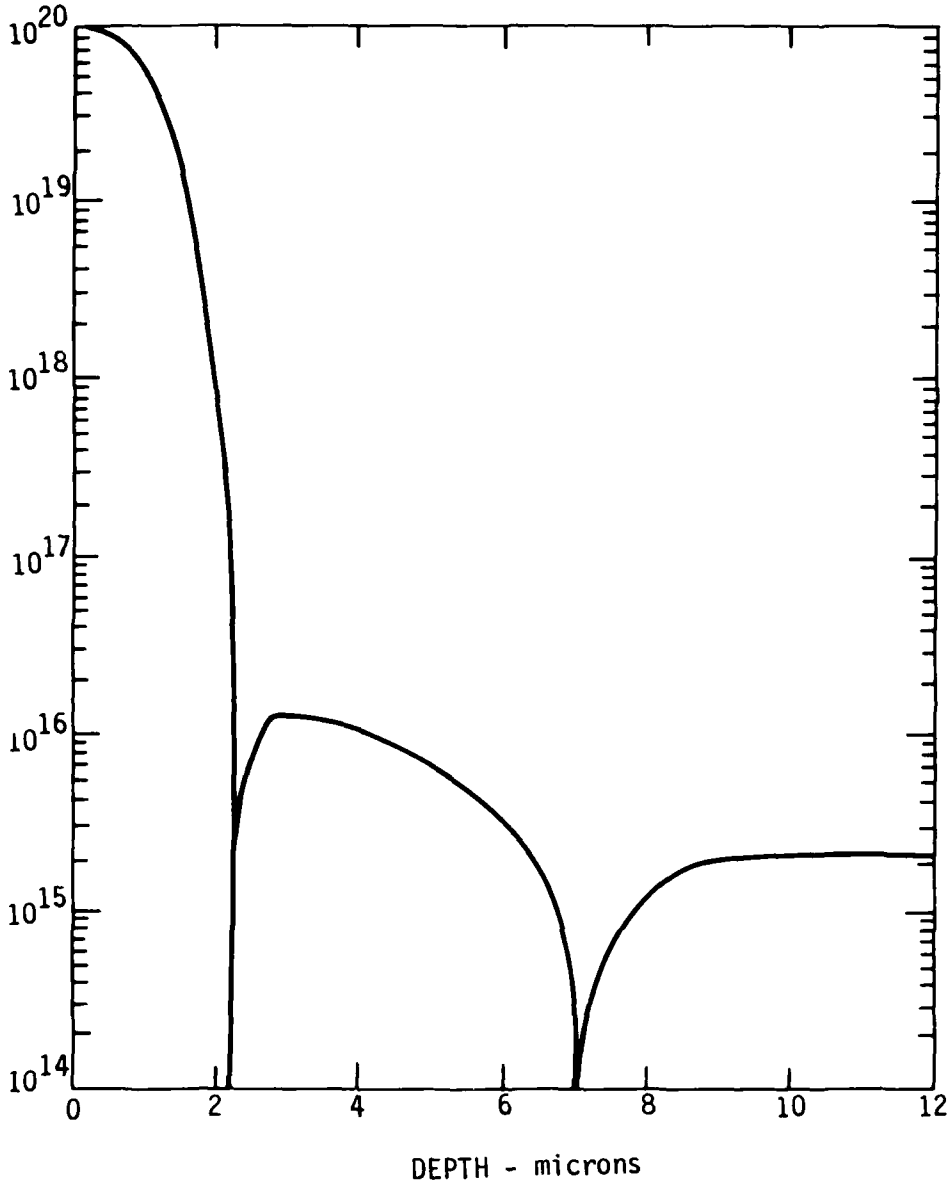


Figure 13. Doping profile of vertical NPN transistor on LATUS test chip.

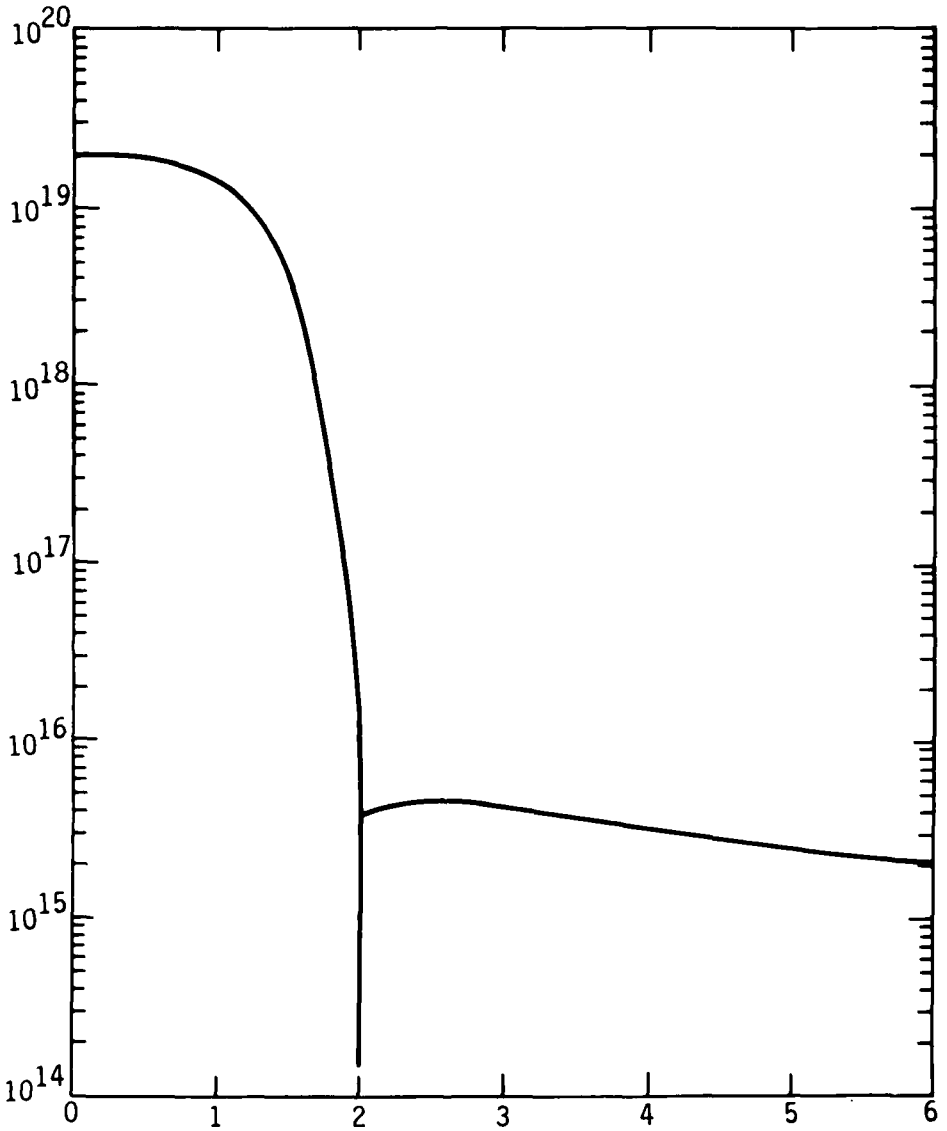


Figure 14. Doping profile of P+ into n substrate on LATUS test chip.

The results of the PN code calculations are shown in Figure 15 along with experimental measurements taken on both non gold-doped and gold-doped wafers. The current gain, β, is plotted versus the collector current I_C. Experimental measurement were taken on structure 36 of subchip A6. The PN code calculations are shown for base lifetimes of 80, 180, 380 and 500 ns.

The experimental data for the non gold-doped device shows a rather constant gain from 10 μA up to where the peak gain occurs (~10 mA). The high current gain degradation is rather gradual out to the highest level measured, 60 mA. The experimental results for the gold-doped wafer shown a greater degradation of gain at lower currents and a more rapid high current gain reduction. The peak gain on the gold-doped devices occurs at a higher current (20-30 mA) than for the non gold-doped device.

The PN code calculations give a peak gain which occurs at about 10 mA with a gradual degradation at 20 mA. Gains at current levels higher than this value are not shown since they demonstrated a very rapid decrease, the reason for which is not presently well understood. The decrease in the calculated gain at the lower currents (<1 mA) show a pronounced reduction which correlates well with the experimental results for the gold-doped devices but not the non gold-doped devices. This degradation at lower currents in the code calculations is probably due to the placement of the single level recombination energy at mid-gap. This maximizes the recombination rate in the emitter-base space charge region. As can be seen from Figure 15, the correlation between the calculated and measured peak gain is very sensitive to the value of base lifetime used. Although there is much data in the literature on minority carrier lifetime in starting material, there is very little information on lifetime in heavily processed silicon such as diffused and/or implanted regions and epitaxial layers. Estreich[6] has measured the lifetime in the substrate material used for the LURIC test chips and found the value to be about 2.5 μs in non gold-doped material. Crystal defects and impurities which result

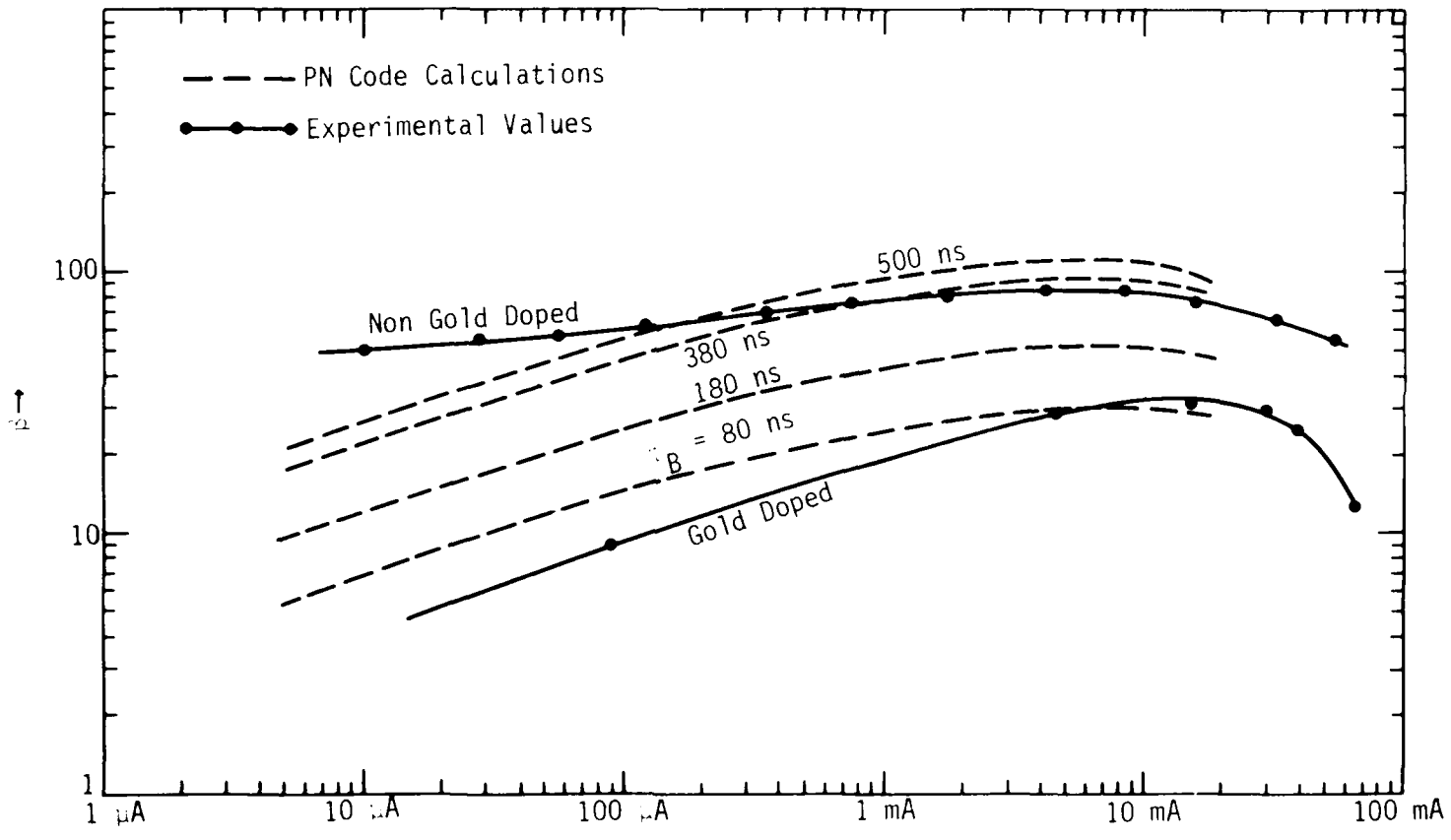


Figure 15. Comparison of τ vs I_c calculated by PN code and measured on a non gold-doped LATUS test chip.

from high temperature processing are known to reduce lifetime, however, the magnitude of the reduction is very process dependent and therefore difficult to estimate. The PN code calculations indicate that base lifetimes are on the order of 350 ns for the non gold-doped LATUS transistor and 80 ns for the gold-doped transistors.

The PN code calculation of gain versus collector current for the LATUS n+, p well, substrate transistor demonstrates that the code can be used to predict the current at which maximum gain occurs but illustrates the sensitivity of peak gain with base lifetime. Without good lifetime estimates, accurate calculations of peak gain cannot be made.

Lateral PNP transistors cannot be modeled accurately with a 1-d code. As demonstrated by Estreich[6], the p+ - substrate - p-well transistor gain must include both a vertical and lateral emitter current term which requires a 2-d code. Therefore no attempt was made to correlate measured lateral PNP gains with PN code calculation. The lateral PNP can be modeled with a composite circuit model which includes both the intrinsic 1-d lateral PNP transistor and a vertical PN diode to simulate current loss to the substrate. This is illustrated in Figure 16.

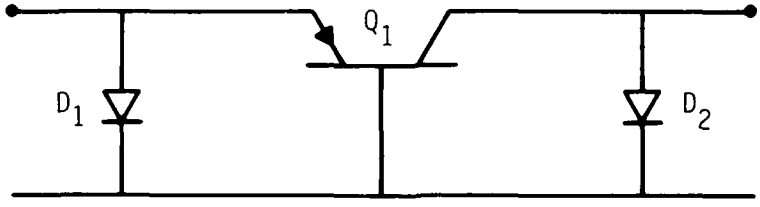


Figure 16. Composite model of lateral p+ - substrate - P well transistor.

The transistor model input parameters for the 1-d lateral PNP transistor can be obtained from a PN code calculation. The diode D_1 is the

P+ - substrate diode and D_2 is the P well substrate diode. Model parameters for D_1 and D_2 can be obtained from PN code calculations for a vertical path through the diodes. The areas of the components are determined from the cross sectional area for lateral current flow in the transistors and vertical current flow in the diodes. This technique has been used to model the lateral PNP injector transistor in I^2L devices.[17]

5.3 CIRCUIT ANALYSIS CODE CALCULATIONS OF PNPN CHARACTERISTICS

The prediction of latchup in integrated circuits is often complicated by the existence of parasitic elements associated with the PNPN structure and by shunt current paths which may drain away sufficient current to prevent the device from latching. Modern computer aided circuit analysis codes can be useful in simulating the PNPN structure in its circuit context and in analyzing overall latchup susceptibility. However, before such analyses can be relied upon, the ability of the code to simulate a latch must be verified. The purpose of the effort described in this section was to evaluate the ability of the SPICE2 circuit analysis program and the models used with it. The reader should note that there are several versions of SPICE available, and the models used in the different versions are not necessarily interchangeable. If possible, the user should examine the subroutines used to implement the bipolar junction transistor model in his version of SPICE. As a minimum, he should use a "curve tracer" program to verify that the transistor simulation matches the intended characteristics. The Sandia Circuit Analysis (SANCA) program* was used in this simulation. It is based on SPICE2E with modifications to permit interactive operation and expanded graphical output.

A PNPN structure can be simulated in SPICE as a cross coupled PNP and NPN transistor as shown schematically in Figure 17. Since the

*SANCA was developed by Dr. G. W. Brown of Sandia National Laboratories.

transistor models in the SANCA version of SPICE do not include avalanche characteristics, a diode has been included across the base-collector junctions to provide the capability to simulate an avalanche initiated latch. With the addition of the diode, the cross coupled transistor model should be able to simulate either gate triggered conduction, avalanche triggered conduction, or photocurrent triggered conduction. The intent of this exercise was to demonstrate these conduction modes and to evaluate the ability of the model to simulate dv/dt effects. No attempt has been made to model any particular PNPN path. However, the NPN transistor parameters have been selected to be similar to those calculated by the PN code for the LATUS devices. The PNP model parameters have been chosen to be reasonable approximations of parasitic lateral PNP transistors. Two NPN models and two PNP models were constructed. The gain versus emitter current characteristic for each is shown in Figure 18. The different transistors were chosen to insure that the holding current variation with gain was properly simulated. The curves in Figure 18 were developed from curve tracer simulations of the individual transistor models. The curve tracer program swept out collector characteristics at base current varying in 9 steps between 1 μA and 4 mA. The user is advised to made such characterizations and plots similar to Figure 18 to serve as an aid to visualizing the conditions necessary for the SCR model to latch.

If the SCR model is constructed with the lower gain NPN transistor and the higher gain PNP transistor, the switching current would be expected to be on the order 35 μA. At this current the gain product of the two devices is approximately equal to one. Figure 19 shows a schematic diagram of the circuit used to test the switching characteristics of the resultant SCR. The anode to cathode voltage was applied through the voltage source V_A. The voltage began at 0 volts for the first 10 seconds of the simulation. It then ramped up to 25 volts over 100 seconds and remained constant for 100 seconds. Finally, it ramped down to 0 volts over 100 seconds and remained constant until the termination of the simulation. The avalanche

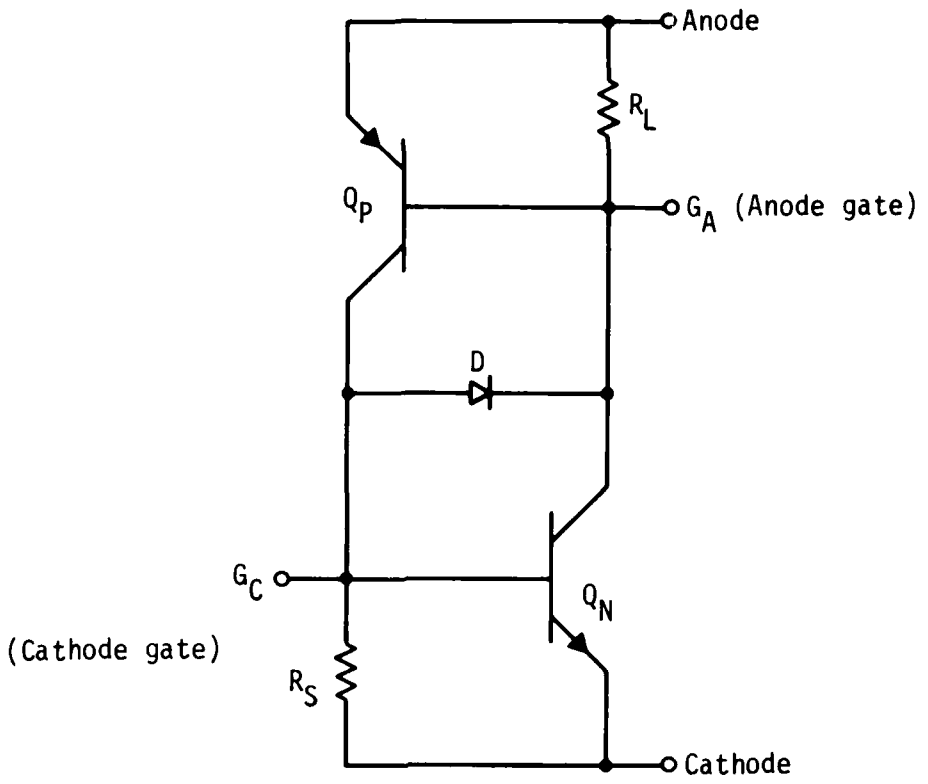


Figure 17. SPICE SCR Model.

diode model simulated a 1 μA current at 20 volts and increased exponentially for higher voltages. The anode resistance was chosen as 101.65 K ohms to limit the current to approximately the value expected for the holding current. The long simulation time was chosen to insure that no dv/dt effects on switching were encountered.

The result of the simulation is shown in Figure 20. The avalanche diode begins clamping the voltage across the SCR model at approximately 20 volts. This voltage remains approximately constant until the supply voltage increase sufficiently to drive current in excess of the holding current through the device. At that point the model simulates latch and the anode to cathode voltage drops to .74 volts. It remains essentially constant at that level until the anode voltage drops so low that the holding current can no longer be supplied. Then the SCR turns off and the anode to cathode voltage rises immediately to the anode voltage.

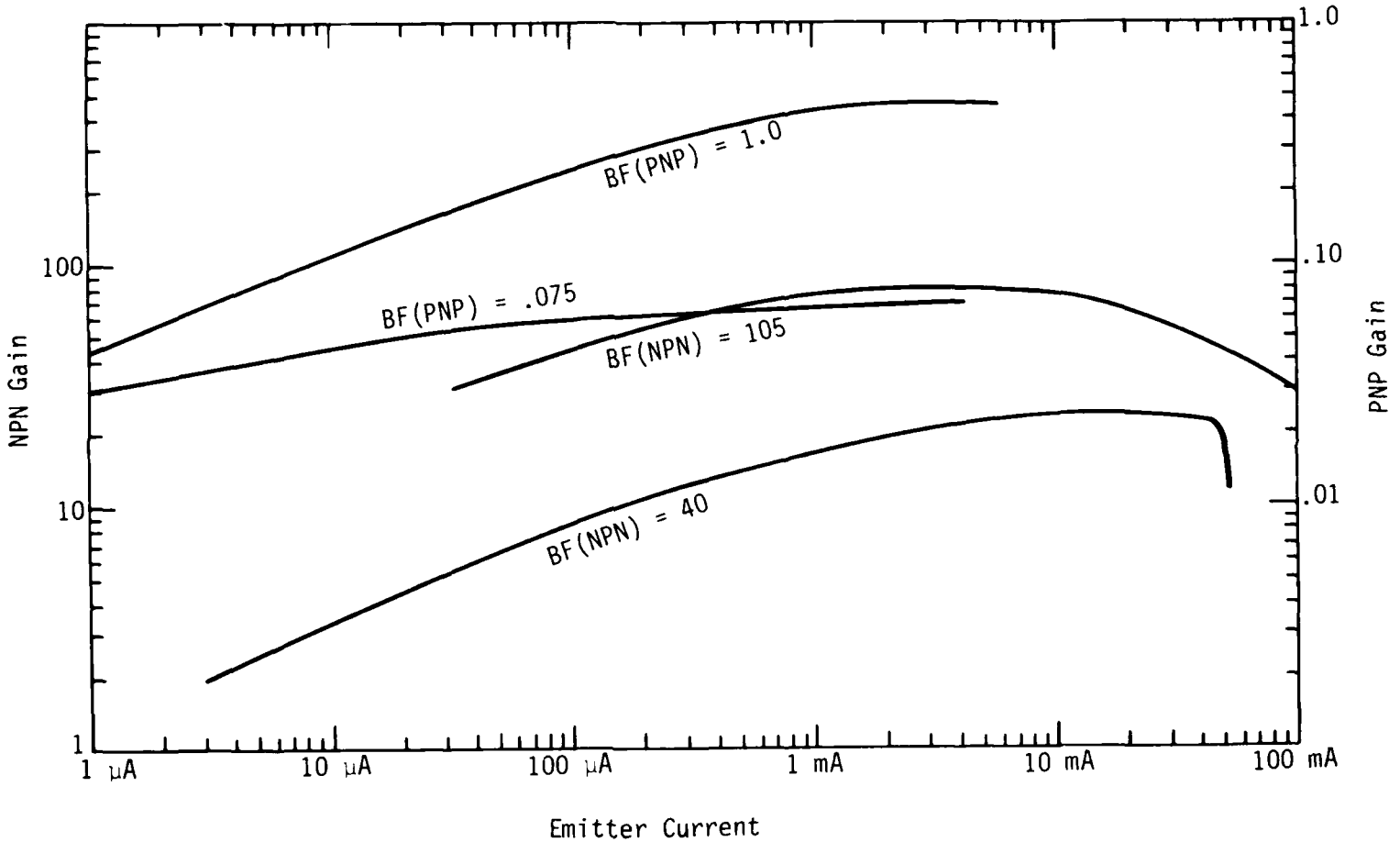
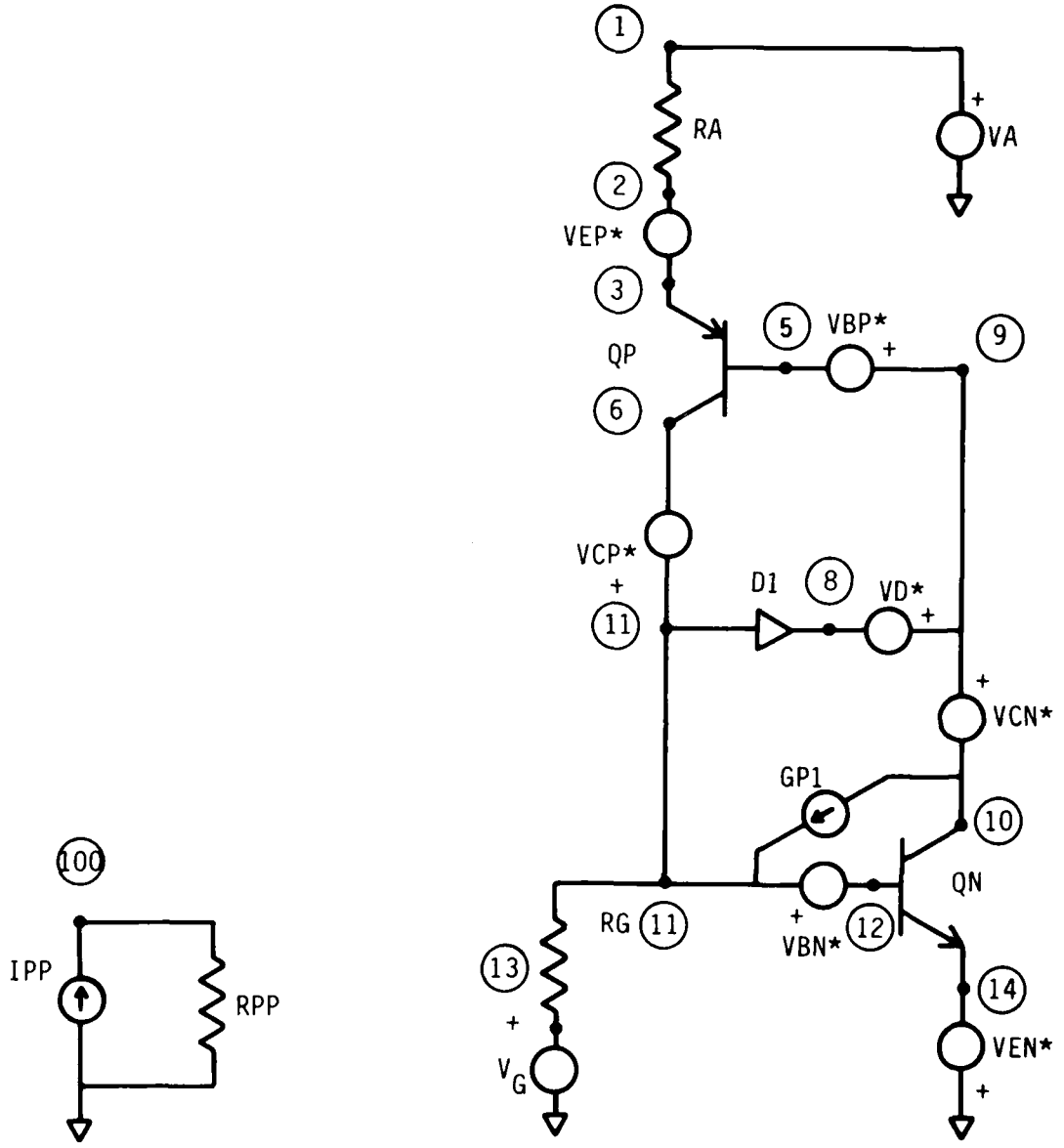


Figure 18. Gain characteristics for NPN and PNP transistor simulations.



*Zero valued voltage sources for current monitoring.

Figure 19. SCR Schematic for SPICE simulation.

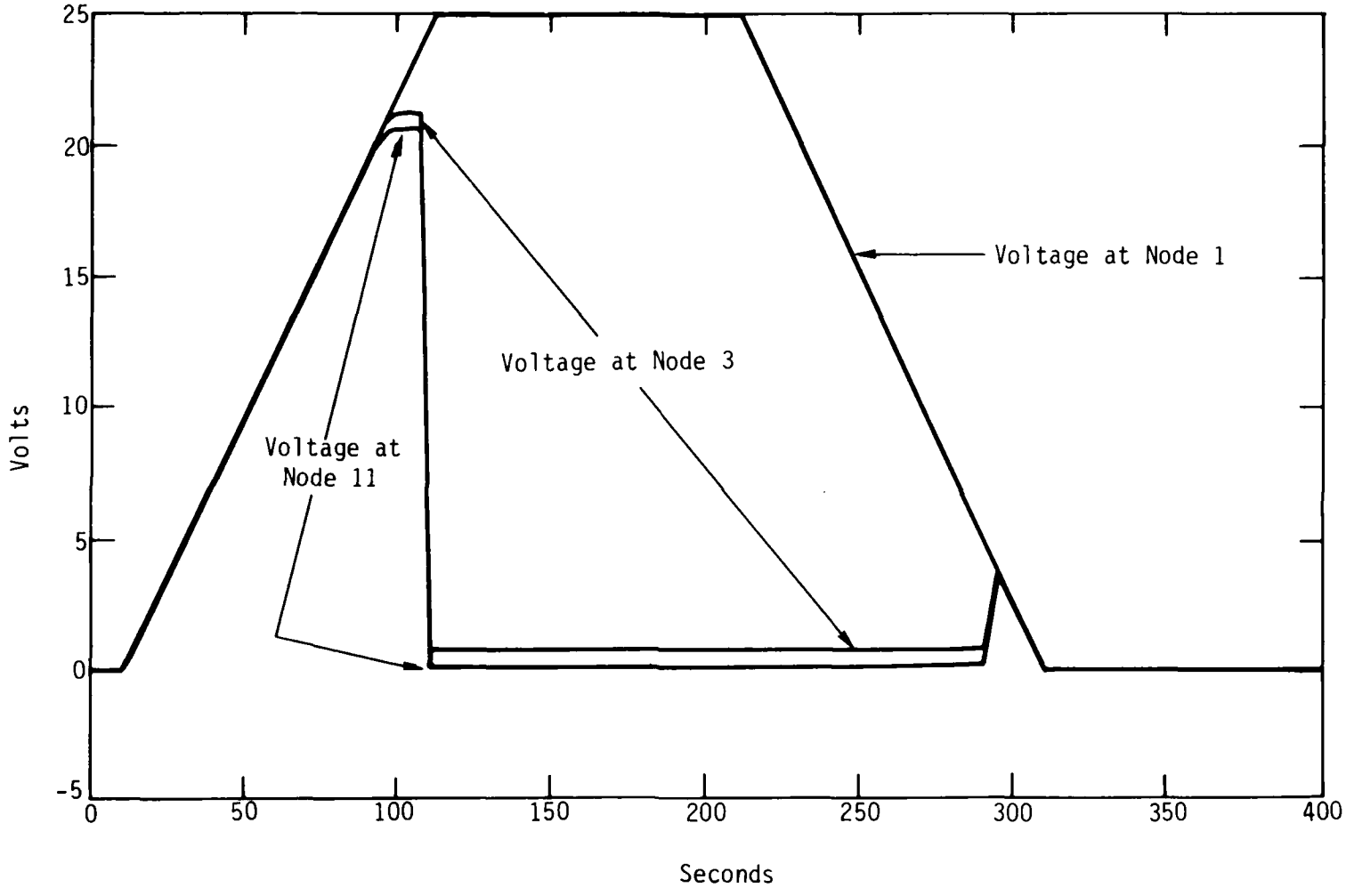


Figure 20. $\beta_{NPN} = 40/\beta_{PNP} = 1$. SCR avalanche triggered switching.

The current/voltage characteristic of the SCR model can be plotted from the solution points of the transient analysis. Figure 21 shows these characteristics in the vicinity of the transition from the negative resistance to the positive resistance region in the on state. Plots have been included for each of three combinations of PNP/NPN models: (1) low gain NPN/high gain PNP, (2) low gain NPN/low gain PNP, (3) high gain NPN/low gain PNP. The expected switching occurred for each combination at currents consistent with those estimated from Figure 18. A DC analysis of the low gain NPN/high gain PNP model was conducted to try to get a more precise estimation of the switching current. It showed that the anode-to-cathode voltage began to drop at a current of 33 μA. No differences were noted between the results of the DC analysis and the transient analysis when the transient simulation time was long compared to the circuit time constants. Also, the I/V characteristic of the SCR when triggered by the cathode gate rather than the avalanching diode was identical to the characteristic shown in Figure 20.

If the ramp time of the anode voltage is decreased, the SCR model should turn on due to dv/dt effects. This is a physically observable effect and is due to the injection of current into the cathode junction as a result of capacitive coupling through the junction capacitances. In the model, the PNP emitter depletion capacitance is in series with NPN emitter depletion capacitance and the parallel combination of the NPN and PNP collector - base depletion capacitances. In addition, each depletion capacitance is in parallel with a diffusion capacitance which is a function of the value specified for parameters TR and TF and the current through the junction. Thus, a manual calculation of the anode voltage transition time necessary to bring about dv/dt triggered switching is difficult. Certainly, an upper bound can be placed by calculating the transition time necessary to provide enough base drive to the base of the NPN transistor to support an emitter current equal to the switching current. In the model using the low gain NPN and the high gain PNP, the switching current is

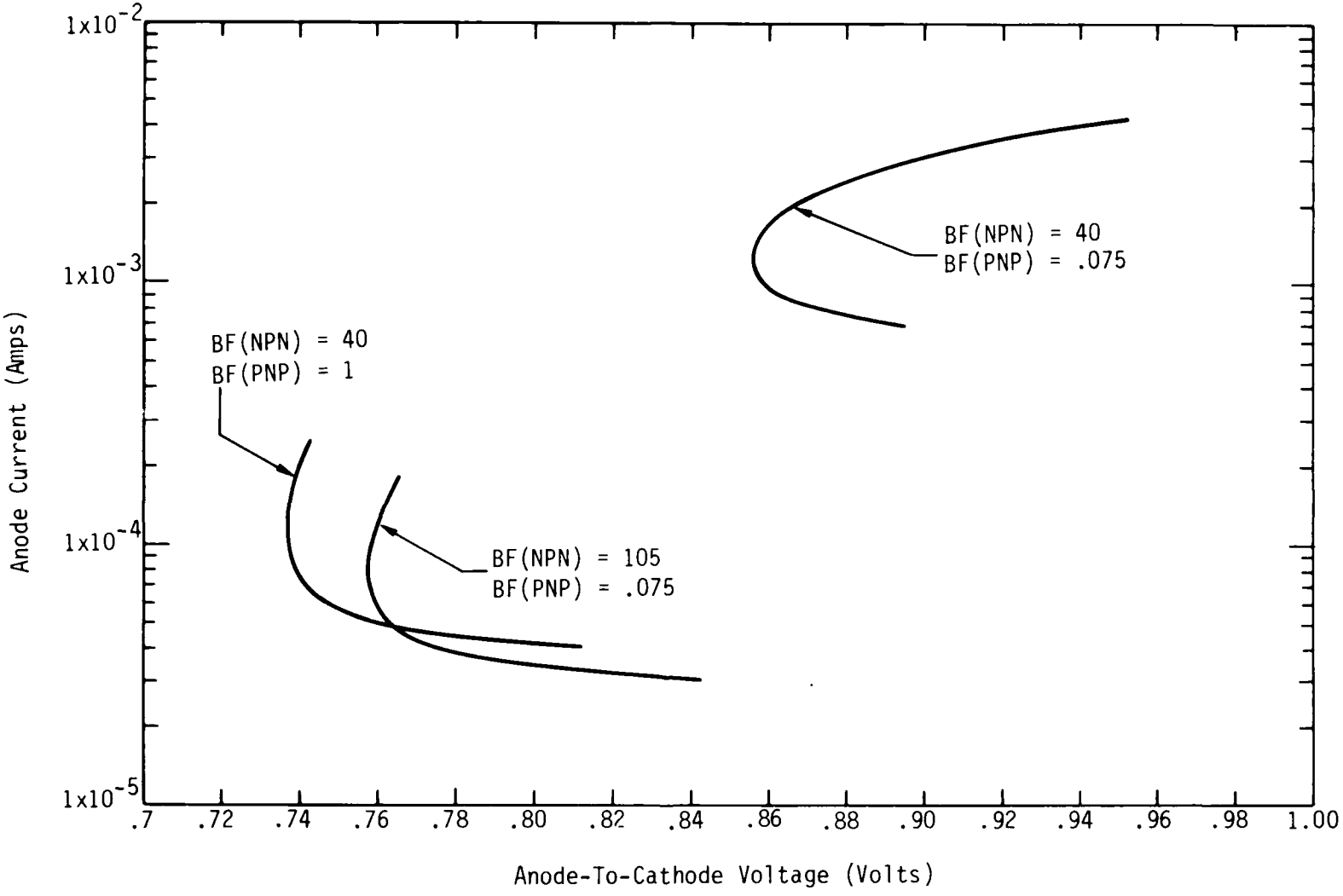


Figure 21. **SCR current/voltage characteristics.**

approximately 35 μA. The gain of the NPN at that emitter current is approximately 5.8. Thus, the required base current is 5.15 μA. Since 0.93 PF is the equivalent capacitance of the series/parallel combination of depletion capacitances, then a transition of 5.5×10^6 volts/sec should trigger dv/dt switching. This is a rough estimate since the SCR model is a regenerative circuit and diffusion capacitances have been ignored.

To examine the actual dv/dt triggering of the model, the transition rate was increased until a dv/dt induced conduction was found. Evidence of the dv/dt effect was observed at 6.25×10^4 volts/sec and a solid switch was observed at 2.5×10^5 volts/sec as shown in Figure 22. The analyst must be very cautious in selecting ramp rates for anode voltages if he does not wish to experience dv/dt switching.

The final triggering mode investigated in this effort was photocurrent induced conduction. Since SPICE does not have a "solve at" feature, photocurrent switching must be investigated in time regimes which are comparable to the photocurrent duration. Otherwise, the SPICE time step will be large and the solution points may not coincide with a time when the photocurrent generator is active. To operate in these short times the bias conditions may have to be supplied to the circuit. If the analyst allows SPICE to calculate the initial conditions, the "on" state of the SCR is often chosen. If the SCR is not meant to be initially conducting, the analyst may either input the required initial conditions or designate one of the transistors in the SCR model as being "off" and allow SPICE to calculate initial conditions. The latter approach was chosen for this exercise. The anode voltage was set at 15 volts and the NPN transistor was designated as off as shown in Figure 23. The independent photocurrent generator IPP was a double exponential source with a 800 ns time constant for both rise and fall and a duration of 4 μs. The amplitude of 20 μA was just sufficient to induce switching as shown in Figure 24. The photocurrent generator has been superimposed on the anode-to-cathode voltage response.

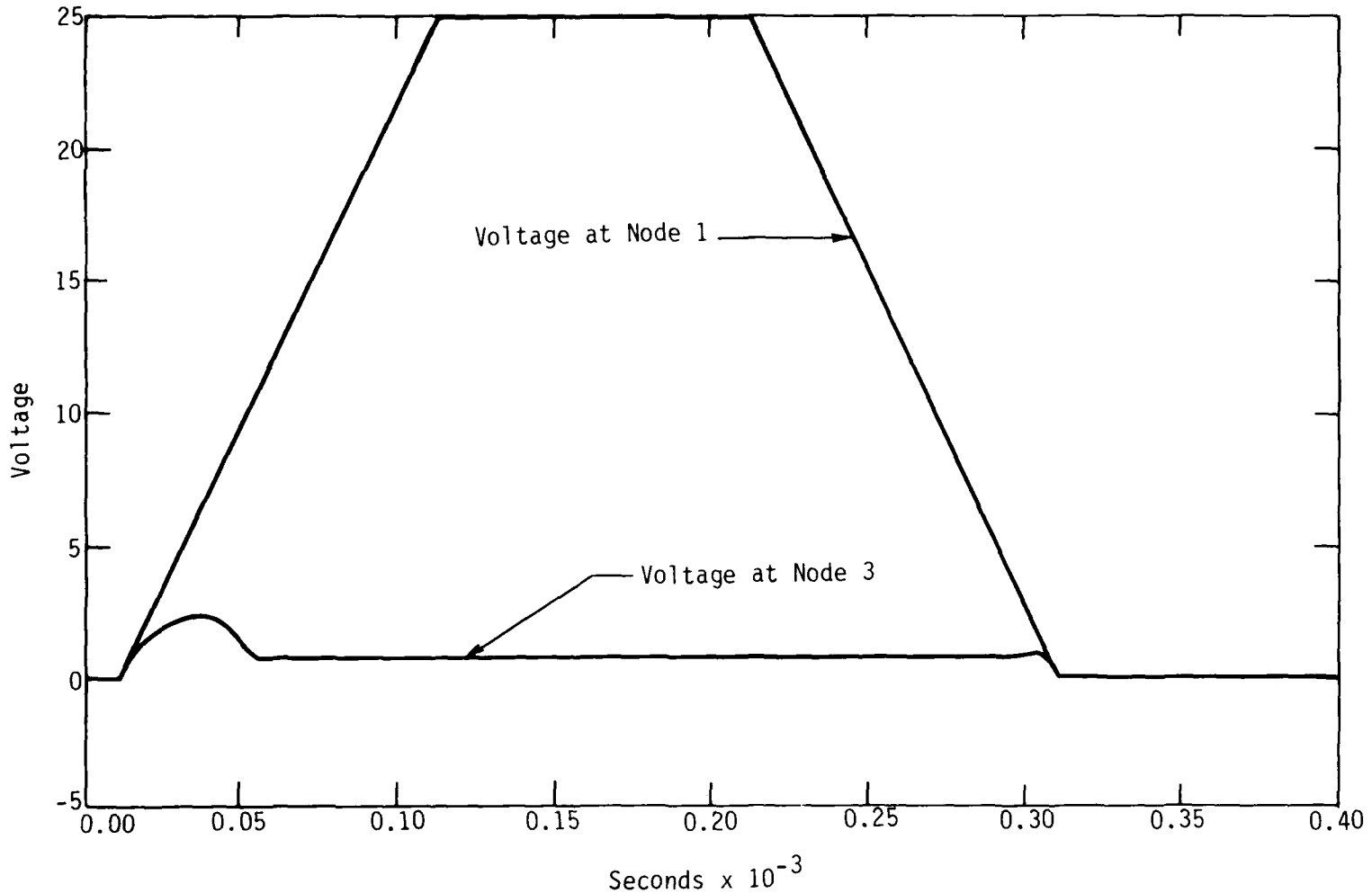


Figure 22. $\beta_{NPN} = 40/\beta_{PNP} = 1$. dv/dt induced switching.

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                                                    *
.L
*****  7-May-82 ******** SANCA  I1.2 ( 1FEB80)  ******** 14:19:37 *****

SCR LATCH

     INPUT LISTING                              TEMPERATURE =   27.000 DEG C

**********************************************************************
 RA 1 2 101.65K
 RG 13 11 1E6
 QP 6 5 3 QP
 QN 10 12 14 QN OFF
 D1 11 8 D
 .MODEL QN NPN(BF=40    BR=1          IS=1E-15
 +             RB=1.8     RC=38         RE=.5
 +             IK=100E-3      C2=4500     NE=1.75
 +             IKR=20E-4     C4=1000      NC=1.8
 +             TF=1NS     TR=1NS        CJE=19.5PF
 +             CJC=39PF)
 .MODEL QP PNP(BF=1.0       BR=1.0        IS=1.0E-15
 +             RB=1         RC=1          RE=1
 +             IK=5M     C2=8000        NE=1.5
 +             IKR=5M   C4=8000        NC=1.5
 +             TF=10NS     TR=10NS         CJE=1PF
 +             CJC=1PF)
 .MODEL D D(RS=1      IS=1E-20     BV=20       IBV=1E-6)
 VEP 2 3 DC 0
 VBP 9 5 DC 0
 VCP 11 6 DC 0
 VEN 0 14 DC 0
 VBN 11 12 DC 0
 VCN 9 10 DC 0
 VD 9 8 DC 0
 *VA 1 0 PULSE(0 25 .00004 .0004   .0004   .0004   .0020 )
```

Figure 23. SANCA listing for SCR photocurrent induced conduction.

```
^L
**********************************************************************
INPUT LISTING                          TEMPERATURE =   27.000 DEG C   PAGE  2
**********************************************************************
 VG 13 0 DC 0
 IPP 0 100 EXP (0 20UA 20US 800NS 24US 800NS)
 RPP 100 0 1
 GP1 10 11 100 0 1
 VA 1 0 DC 15
 .TRAN 1E-6  100E-6
 *.TRAN 500N 100US
 *.DC VA 0*.0 25*.0 1*.0
 .PLOT TRAN V(1) V(3)
 .PLOT TRAN I(VA) I(VBN)
 .PLOT TRAN V(100)
 .PRINT TRAN V(1) V(3) I(VA) I(VEN)
 .PRINT TRAN V(5) V(11) V(11,8)  I(VCN) I(VBN)
 .END
*
```

Figure 23. SANCA listing for SCR photocurrent induced conduction (Concluded).

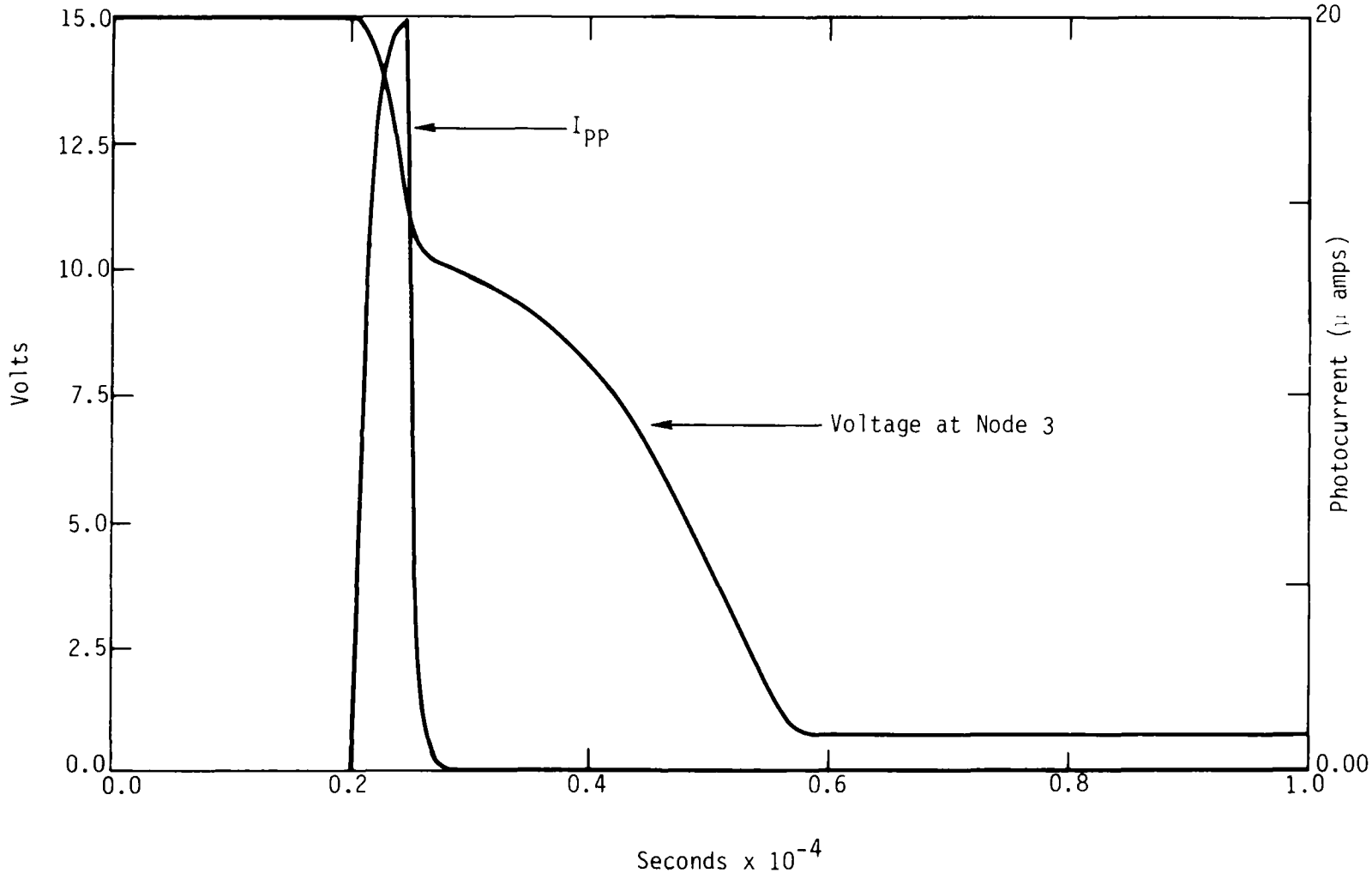

Figure 24. $\beta_{NPN} = 40/\beta_{PNP} = 1$. Photocurrent triggered conduction.

The anode-to-cathode voltage switches to an intermediate level during the photocurrent and continues to a fully on state after the photocurrent is switched off.

The results of this investigation indicate that the SPICE SCR model is suitable for simulating latchup effects. However, great care must be taken to insure that the gain characteristics of the models are consistent with the latchup characteristics being simulated. Also, the analyst must be aware of dv/dt induced switching and the necessity for specifying and transistor as off when permitting SPICE to calculate initial conditions on a biased circuit.

5.4 1-d Code Calculations of PNPN Characteristics

The PN code can be used not only to calculate diode and transistor characteristics, but characteristics of multilayer structures up to six layers. The use of the PN code to study PNPN structures was demonstrated by IRT[7]. The major limitation in calculating SCR characteristics is the one-dimensionality of the code and the fact that only three of the four regions can be accessed by an external connection. This limits the number and configuration of parasitic elements that may be attached to the SCR terminals. A possible advantage to the use of the PN code applied to the four layer structure is that the physics of the SCR response is inherently included in the calculations. Therefore, the feedback mechanism is taken care of internally and "effective" gains are automatically used in calculating response characteristics. Another advantage is that generation of carriers by external radiation can be included in the code, hence the PNPN response to a dose rate environment can be more realistically simulated.

As a first test of the ability of the PN code to simulate parasitic PNPN response in a bipolar LSI device, a PNPN path in the AD571 was chosen. The anode is the collector of a lateral PNP (Q320) and the cathode the

emitter of a vertical NPN (Q315) in the same isolation region. A one dimensional path was chosen and dimensions were taken from a photomicrograph of the region. The doping profile was constructed from angle lap data taken by NWSC Crane and resistivity data supplied by the vendor (Analog Devices). The profile is shown in Figure 25. This profile, which is known to have a $\beta_P \cdot \beta_N >> 1$, was used primarily to explore the capability of the code to demonstrate bistable action under a variety of conditions. No avalanche parameters were input to the code and a single level recombination model was used with the energy level set at midgap. Triggering of the SCR was attempted by applying a cathode gate pulse and by a simulated radiation pulse. In both cases a current limiting load resistor, R_L, was placed in the anode lead and the potential across the SCR and R_L was ramped from 0V to 30V in 10 μs and held at 30V. Gate triggering was performed by ramping the gate potential to 1V across a 100 Ω shunt resistance, R_S, to inject a large current (10 mA) into the NPN base. The circuit diagram for this simulation is shown in Figure 26. The gate potential was maintained for 100 μs then removed. The SCR switched on and remained on after the gate pulse was removed, demonstrating that bistable operation could be simulated with a gate trigger. Triggering by transient radiation was demonstrated by applying a 500 ns pulse of $\sim 10^{10}$ rad(Si)/sec to the SCR in the off state. The circuit diagram for this run in shown in Figure 27. The device switched to the on state and remained on after the radiation pulse was removed. In the PN code the radiation pulse is simulated by a uniform increase in carrier density proportional to the applied dose rate throughout the four layer structure. These results verify the capability of the code to predict bistable operation in a bipolar LSI parasitic four layer structure with a known β product much greater than one. This demonstration is not surprising since bistable operation of a four layer device was shown for the PN code in an earlier study for a uniform doping profile.[7]

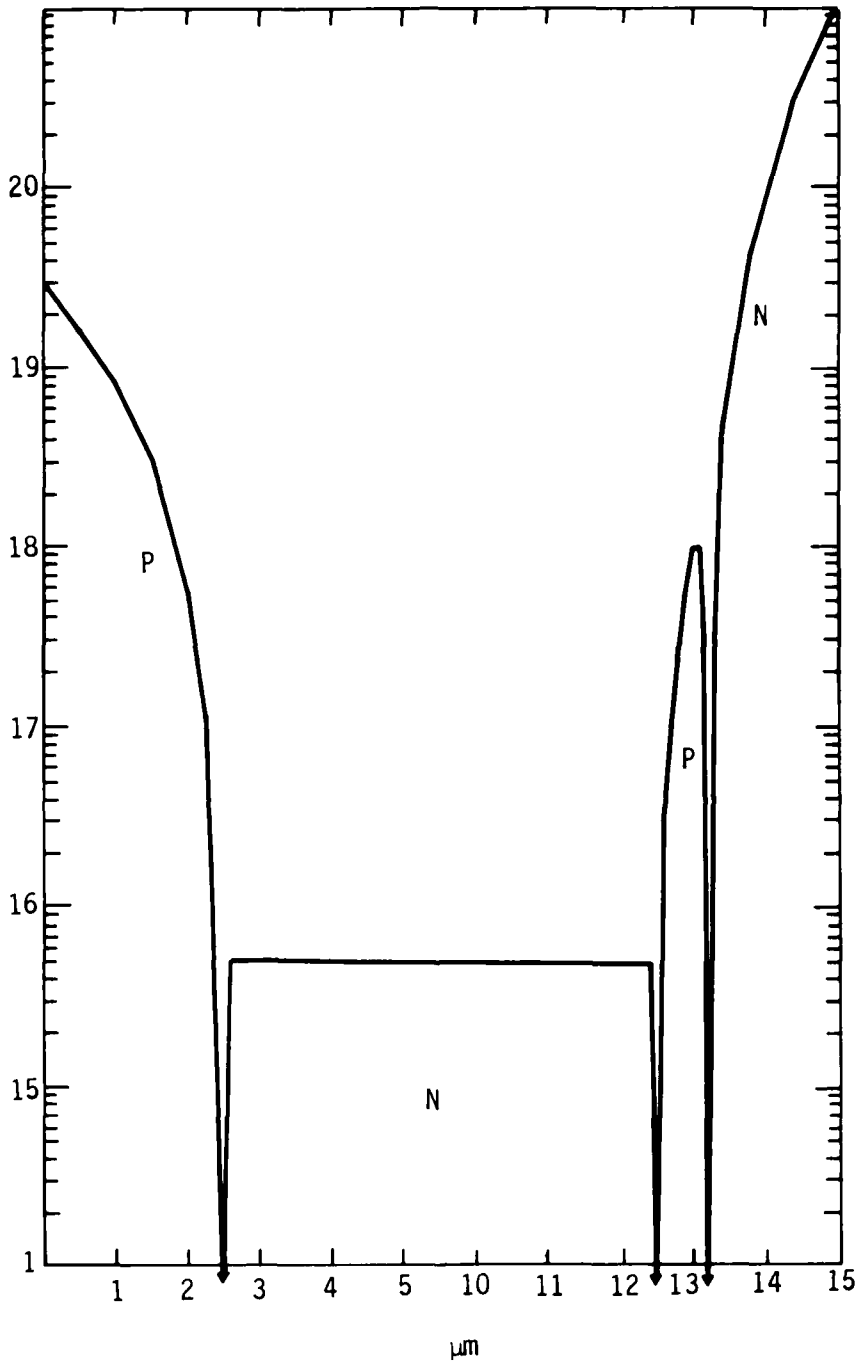

Figure 25. Doping profile for PNPN path in AD571.

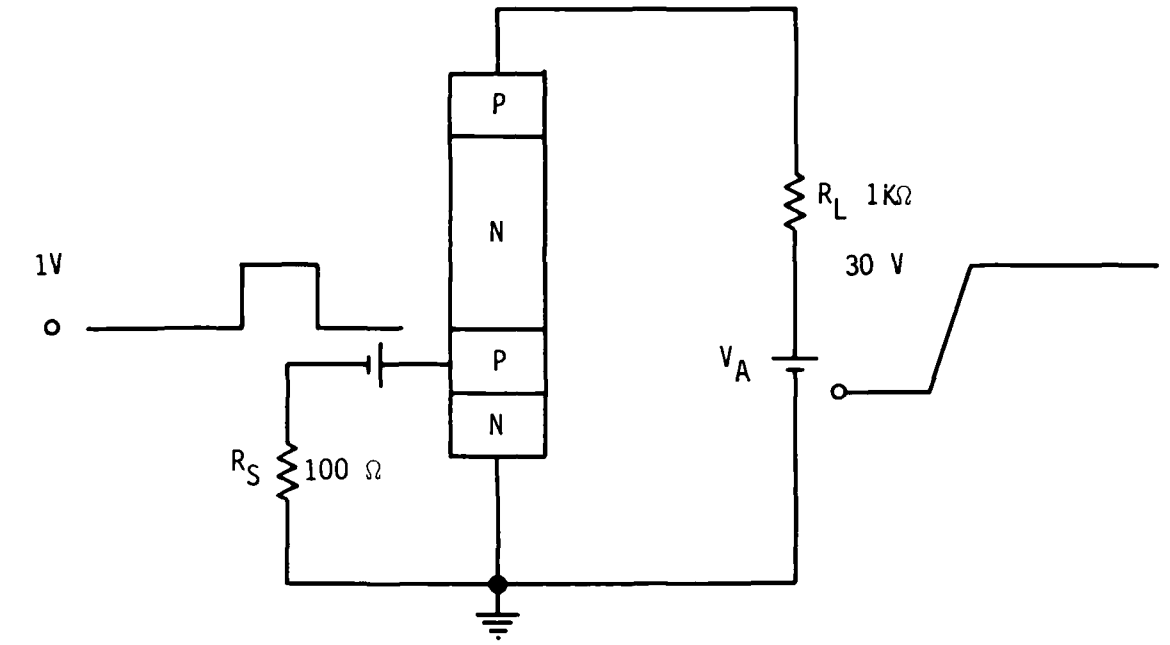

Figure 26. PN code circuit diagram for gate triggering of AD571 pnpn path.

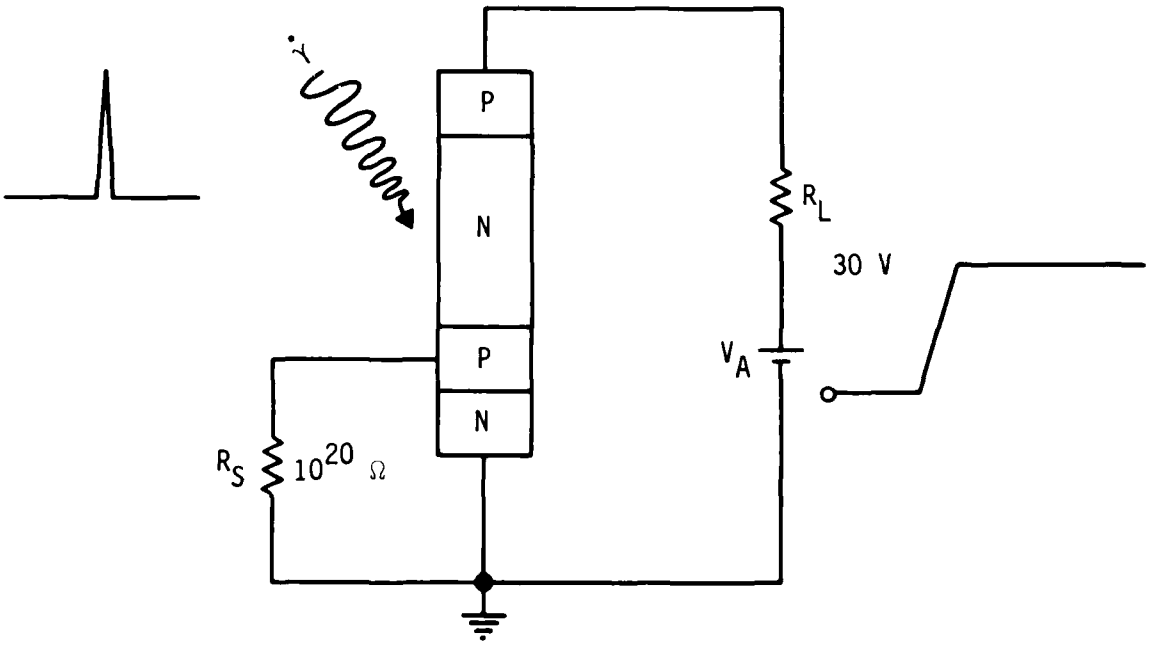

Figure 27. PN code circuit diagram for $\dot{\gamma}$ triggering of AD571 PNPN path.

A much more stringent test of the predictive capability of the code is the calculation of holding current and holding voltage for a path known to latch and the prediction of no latchup for a structure with a known β product very close but less than one.

In order to determine the holding current, the current available to the anode must be systematically reduced until the SCR begins to turn off. There are several ways to demonstrate switching from the on to the off state by reducing the current. In this study the method used was to slowly decrease the anode supply voltage. Since in the on state the load resistor and anode supply voltage act as a current source, the current can be reduced either by reducing R_L or V_A. R_L cannot be changed during a single run. Therefore reducing R_L would require a separate run for each reduced value. V_A can be ramped from its maximum value to OV during a single run. However, if the holding current is less than $(V_A-V_H)/R_L$, then the holding current cannot be calculated. This is due to the fact that at least V_H is required to maintain the SCR on and once V_A approaches V_H, the SCR begins to turn off due to voltage limitation. Therefore, in order to adequately predict the holding current, the value of R_L must be chosen such that the current limited to the SCR in the on state is just slightly greater than I_H. This requires an interactive procedure with perhaps several runs. Computer costs can be significantly reduced in this process by using data from a previous run rather than starting from scratch each time.

Holding voltage is determined from the same I-V switching characteristic used to determine I_H. V_H is the minimum value of anode to cathode voltage, V_{AK}.

A partial demonstration of the determination of I_H was performed on the parasitic PNPN structure from the AD571. Using the gate triggering circuit, shown in Figure 26, the SCR was triggered into the on state and

after holding V_A at 30V for 100 μs while the SCR was in the on state, V_A was reduced linearly from 30V to 0V in 50 μs. Switching occurred at 25.5 μs from the start of the ramp. The anode current was approximately 13.5 mA. This is the value of holding current for the particular circuit configuration shown in Figure 26, where the shunt resistance is 100 Ω.

Another demonstration of holding current evaluation was performed using a shunt resistance of 1 K Ω and triggering by dose rate. In this case the load resistance was again 1 K Ω giving an I_A(MAX) of ~30 mA. The PNPN structure did not start to come out of the latch until the V_A had been lowered to ~1.75 V at which point I_A was between 700 and 800 μA. These two runs illustrate that the PNPN structure can be switched from the on to the off state by lowering I_A to a value lower than the holding current. In both of these cases the holding current is determined by the value of R_S since the V_{BE} of the NPN transistor must be maintained at about .7V by the IR drop through R_S for the SCR to remain on. Thus I_H is inversely proportional to R_S. What is of primary interest in a latch-up analysis is the worst case value of holding current which occurs when $R_S = \infty$. In this case holding current is determined by the minimum value of anode current for which the product gains ($\beta_N \cdot \beta_p$) equals one.

An attempt was made to determine the worst case holding current for the AD 571 profile. Worst case is obtained with the gate open which was simulated with $R_S = 10^{20}$ Ω. Since the parasitic transistor gains were very large for the AD571 PNPN profile, the gains were reduced by degrading the lifetime so that the product gains would be less than one at some realistic current level. Several combinations of lifetime, τ, and load resistor, R_L were used. The technique used to calculate holding current was to apply an anode voltage, V_A, of 30 V, trigger the SCR on with dose rate, then slowly ramp V_A to 0V and observe the I-V characteristic. A plot of the calculated I-V characteristic is given in Figure 28 for three

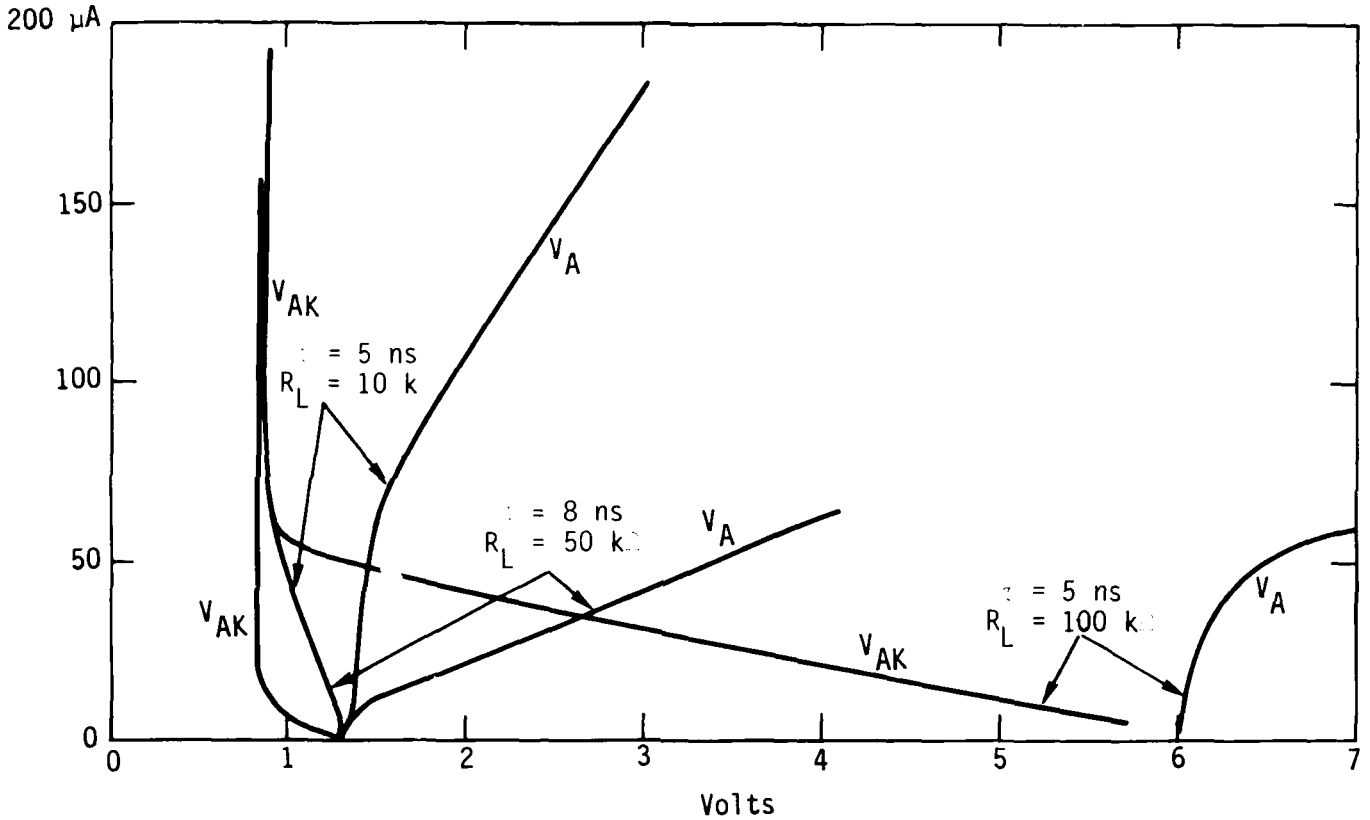

Figure 28. Anode current vs applied voltage (V_A) and anode to cathode voltage (V_{AK}) for various load resistors and lifetimes on AD571 PNPN profile.

different runs. The anode current I_A is plotted vs the applied voltage V_A and the actual anode to cathode voltage V_{AK}. As can be seen from the plots, the choice of τ = 5 ns with a load resistor of 100 KΩ displays a sharp switching characteristic from the on state to the off state as V_A, hence I_A, is reduced. For this case the holding current is between 50 and 60 μA and the holding voltage is about .9V. With a load resistor of 10 KΩ, the τ = 5 ns characteristic is much more gradual and the holding current and voltage are more difficult to determine. Also the τ = 8 ns, R_L = 50 KΩ curve does not show a sharp transition but I_H and V_H can be determined. With τ = 8 ns, I_H is between 10 and 20 μA. These calculated I-V characteristics demonstrate that the PN code can be used to determine a worst case I_H and V_H using the techniques of ramping I_A from a value of V_A/R_L to zero if R_L is chosen such that $I_H >> (V_A - V_H)/R_L$.

Since the calculation of holding current on the AD 571 profile was made with a degraded lifetime, no comparisons to experimental data are possible. However it is useful to determine the correlation between the holding current calculated in this manner and the holding current that would be calculated from the product gains of the parasitic transistors. In order to make this comparison, the individual PNP and NPN profiles for the AD571 PNP structure were run on the PN code to calculate the gain vs emitter current using a lifetime of 5 ns. Both the NPN and PNP gains are plotted vs the emitter current and the resultant product calculated. The lowest current for which $\beta_N \cdot \beta_p = 1$ was 23 μA. This is about a factor of 2 lower than the holding current as determined by ramping the anode current on the PNPN structure. This discrepancy can probably be explained either by the different boundary conditions on the profiles used in making the computations or the difference between effective gain and terminal gain. Whatever the reasons may be to account for the difference, the agreement between the holding current calculations for these two diverse approaches

is quite good. These results demonstrate the capability of the PN code to reproduce SCR characteristics.

As mentioned, no attempt was made to obtain quantitative results on the AD571 profile. However, an attempt was made to quantitatively characterize the LATUS test structures on the LURIC test chip. The doping profile for these structures was shown in Figures 13 and 14. PNPN profiles were obtained for PN code inputs by considering two different one dimensional paths shown in Figure 29. The profiles of these two paths are very different. A qualitative argument can be made from the actual dimensions of the various regions, that, due to current spreading, the most likely path is path 2, even though it is somewhat longer than path 1. However both paths were modeled and profiles input to the PN code.

As discussed in a previous section, there are two types of LURIC test chips available, one gold-doped to kill lifetime and the other non gold-doped. Actual measurements on the A5 and A6 subchip LATUS tests structures indicated that all four would latch. However, for the gold-doped wafers, the holding currents were rather high as would be expected due to the degradation of lifetime. Table IV is a list of the holding currents and voltages measured for the four structures.

Table IV

Wafer 2204A Gold-doped 50 Å

Structure	Subchip	W_B	I_H	V_H
	n			
29	A5	10 μm	1.4 mA	~1V
30	A5	20 μm	17 mA	~3V
35	A6	30 μm	37 mA	~5V
36	A6	50 μm	63 mA	~8V

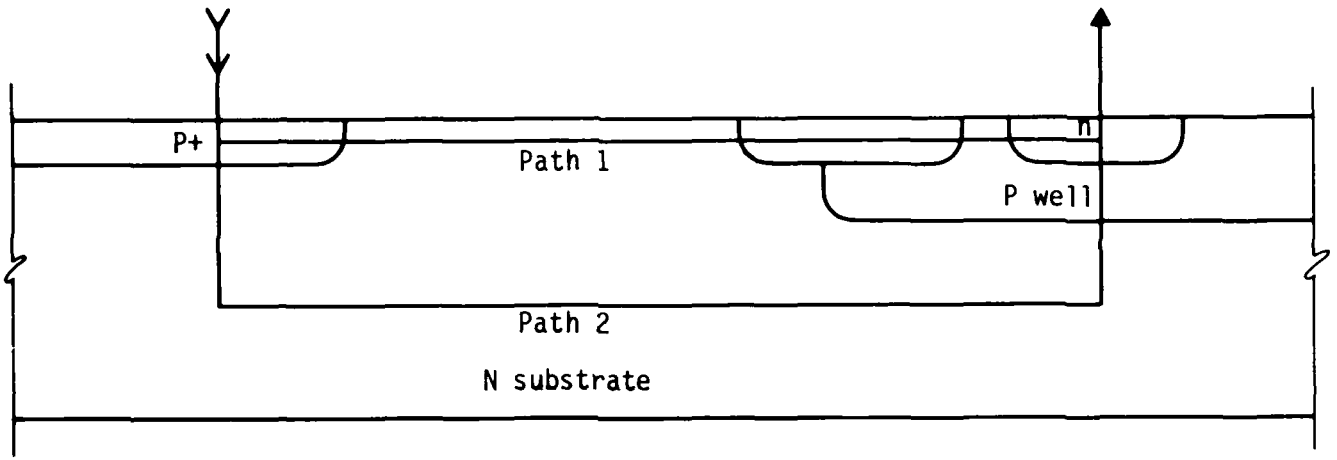

Figure 29. Two one dimensional PNPN paths through LATUS test structure.

In order to calculate the holding current for these structures, an appropriate value of lifetime is required. Using the expression for calculating the gain of a lateral transistor given in Section 5.1 and data taken for a lateral PNP with W_B = 64 μm, a lifetime of 100 ns was calculated. This would correspond to a gold concentration of about 5 x 10^{14} cm^{-3}.

With τ = 100 ns and using path 2 for structure 36, the simulated 1-d PNPN profile was easily latched using dose rate triggering. The maximum applied V_A was 15 V and the load resistor 10^4 Ω which limits the current to about 1.5 mA. This current is well below the measured holding current of 63 mA. The anode to cathode voltage with an anode current of 1.4 mA was calculated to be 1.01 volts which is well below the measured holding voltage of 8 V. The applied voltage was ramped to 0V to determine at what current the SCR would turn off. The anode to cathode voltage continued to decrease without a turnaround.

These results indicate that the 1-d PN code simulation of the LATUS PNPN path does not correlate with the measured characteristic. Although an actual value of I_H was not calculated in the simulation, its value is known to be well below 1 mA compared to a measured I_H of 63 mA. Also the calculated V_H was 1V compared to a measured value of 8 V. The failure of the simulation is due to the limitations of the 1-d code to simulate 2-d current flow. As seen from the cross section of the LATUS structure, Figure 29, current injected into the p+ anode region will have both a vertical and lateral component. This is the basis of the analytical expression derived by Estreich for the gain of a lateral transistor. The PN code simulation ignores the current loss to the substrate because of the 1-d limitation. This vertical component of current loss to the substrate greatly reduces the effective PNP current gain and hence increases I_H significantly. The high value of V_H measured experimentally is most likely due to the resistance of the PNP base region. The n substrate has a resistivity of 2.5 Ω cm and the base region is 40 μm wide. Assuming current flow is

limited to a cross sectional area of twice the area defined by the width of the p well times its depth, the resistance of the PNP base is 270 Ω. With an anode current of 63 mA through this region, one would expect a voltage drop of 17 V. Since the measured holding voltage was only 8 V, then either the base resistance was lowered by conductivity modulation or the cross sectional area of current flow was about twice what was originally estimated. Therefore, it appears that the low value of V_H calculated by the PN code was simply due to the low value of holding current predicted by the code.

The attempt to obtain quantitative calculations of I_H and V_H using the PN code to simulate a 1-d PNPN structure has demonstrated that the one dimensionality of the code makes it totally inadequate for obtaining good correlation with measured results. Although this result was only verified for a gold doped (i.e., short lifetime) case, similar results can be expected for longer lifetime, non gold doped devices since the parasitic gains and hence holding currents will scale down with increased lifetime. However, it has been demonstrated that the PN code can be used to reproduce an SCR I-V characteristic, from which a value of I_H and V_H can be derived.

6. RADIATION INDUCED LATCHUP TESTS

Latchup testing was performed on the 9408 and AD571 at White Sands Missile Range using the Nuclear Effects Lab LINAC facility. No tests were performed on the SBP9900A since it was concluded that latchup could not occur in nonisolated I^2L. Five 9408 circuits were tested at a V_{CC} of 5 V with all inputs both high and low and with all outputs both high and low. The AD571 is available in two versions, the AD571K which is CMOS compatible and can be operated with V_{CC}^+ = 15 V, and the AD571J which is T^2L compatible and is operated with V_{CC}^+ = 5 V. Seven AD571Js and five AD571Ks were tested using the worst case bias conditions established by the detailed circuit analysis prior to discussions with Analog Devices.

The LINAC was operated in the electron beam mode with an electron energy of 20 MeV. Each device was tested at a dose rate of 10^9 and 10^{10} rad(Si)/sec with a 100 ns pulse width and at 10^9 and 10^{10} rad(Si)/sec with a 1 μs pulse width. This gave a range of 100 rad(Si) per pulse to 10 Krad(Si) per pulse. Power supply surge currents were monitored during each pulse.

The 9408 was operated in a static DC condition with the inputs and outputs preset to establish the range of bias conditions. The occurrence of latchup was monitored by observing the supply current and surge currents. The nominal supply current was 140 mA and the supply was current limited to ~300 mA. A bypass capacitor of 10 μF was used to provide a current source during the pulse. The AD571 was operated at 10 kHz and the data ready line monitored to assure that the circuit was going through a conversion. None of the output bits were monitored during the test. The V_{CC}^+ and V_{CC}^- supplies were current limited to 200 mA to prevent burnout if latchup occurred. Latchup was monitored by observing the supply currents, the surge currents and the data ready line.

The results of the latchup tests were that no latchup was observed in any of the test devices under any of the dose rate, pulse width or bias conditions.

After discussions with Analog Devices concerning the latchup path in the bipolar offset circuit, and detailed SPICE simulations of the latchup, additional radiation induced latchup tests were performed. In these tests, performed by NWSC Crane using a pulsed laser, the input voltage was varied and all bits read before and after the radiation pulse. Again no latchup was observed up to dose rates of 10^{10} rad(Si)/sec.

The 93471 units were latchup tested by Boeing Aerospace on their LINAC facility under contract to NWSC Crane. In these tests both wide (1 μs) and narrow (30 ns) pulse testing was performed at dose rates between 10^{9} and 10^{10} rad(Si)/sec both at room temperature and at 70° C. Again, no latch-up was observed under a variety of test conditions.

REFERENCES

1. Crowley, J. L., F. A. Junga and T. J. Stultz, "Technique for Selection of Transient Radiation-Hard Junction Isolated Integrated Circuits," IEEE Trans. on Nuc. Sci., Vol. NS-23, No 6, December 1976.

2. "Integrated Circuit Latchup Analysis Procedure," first draft in ASTM subcommittee F1.11 for review.

3. Ochoa, A. Jr. and P. V. Dressendorfer, "A discussion of the Role of Distributed Effects in Latch-up," IEEE Trans. on Nuc. Sci., Vol. NS-28, p. 4292, December 1981.

4. Phillips, A. V., Transistor Engineering, McGraw Hill, New York, 1962.

5. Sze, The Physics of Semiconductor Devices, John Wiley and Sons, New York, 1969.

6. Estreich, D. B., "The Physics and Modeling of Latch-up and CMOS Integrated Circuits," Technical Report G-201-9, Stanford University, November 1980.

7. Leadon, R. E. and M. L. Vaughn, DASA 2358, Final Report on Contract DAS01-68-C-0123, June 1969.

8. Nagel, L. W. and D. O. Penderson, ERL, University of California, Berkely Memo ERL-M382.

9. Goldthrop, D. C. and E. B. Slutsky, "An Integrated Circuit Composite PNPN Diode," Presented at 1979/EDM.

10. Raymond, J. P., T. Y. Wong and K. K. Schuegraf, "Radiation Effects on Bipolar Integrated Injection Logic," IEEE Trans. on Nuc. Sci., Vol. NS-22, December 1975.

11. Raymond, J. P., and R. L. Pease, "A Comparative Evaluation of Integrated Logic," IEEE Trans. on Nuc. Sci., Vol. NS-24, December 1977.

12. Brokaw, A. P., "A Monolithic 10-Bit A/D Using I^2L and LWT Thin Film Resistors," IEEE Journal of Solid State State Circuits, Vol. SC-13, No. 6, December 1978.

13. Scharfetter, D. L., Solid State Electronics 8, 299, 1965.

14. Cooper, M. S., J. P. Retzler and G. C. Messenger, "High Temperature Schottky TTL Latchup," IEEE Trans. on Nuc. Sci., Vol. NS-25, December 1978.

REFERENCES (Concluded)

15. Kroell, K. E., "Parasitic SCR Between a Schottky Diode and an Adjacent Transistor," Solid State Electronic 19, 711, 1976.

16. Matthews, W. H., R. P. Mertens and J. D. Stulting, IEEE, ED-24, p. 1228-1233, October 1977.

17. Pease, R. L., "Analytical Investigation of Neutron Hardening of Integrated Injection Logic," IEEE Trans. on Nuc. Sci., Vol. NS-27, p. 1396, December 1980.

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DEPARTMENT OF ENERGY

Department of Energy
Albuquerque Operations Ofc
ATTN: WSSB
ATTN: WSSB, R. Shay

OTHER GOVERNMENT AGENCIES

Central Intelligence Agency
ATTN: OSWR/NED
ATTN: OSWR/STD/MTB
ATTN: OSWR, T. Marquitz

Department of Transportation
Federal Aviation Admin
ATTN: ARD-350

NASA
ATTN: M. Baddour

OTHER GOVERNMENT AGENCIES (Continued)

NASA
ATTN: Code 311.3, D. Cleveland
ATTN: Code 654.2, V. Danchenko
ATTN: Code 724.1, M. Jhabvala
ATTN: Code 5301, G. Kramer
ATTN: Code 710.2, D. Haykin, Jr
ATTN: Code 601, E. Stassinopoulos
ATTN: Code 660, J. Trainor
ATTN: Code 310, W. Womack
ATTN: Code 695, M. Acuna
ATTN: Code 701, W. Redisch
ATTN: Code 311A, J. Adolphsen

NASA
ATTN: EG02
ATTN: H. Yearwood
ATTN: M. Nowakowski

NASA, Headquarters
ATTN: Code D, W. McInnis
ATTN: Code DP, B. Bernstein
ATTN: Code DP, R. Karpen

Department of Commerce
National Bureau of Standards
ATTN: Code A327, H. Schafft
ATTN: Code A305, K. Galloway
ATTN: C. Wilson
ATTN: R. Scace
ATTN: T. Russell
ATTN: Code C216, J. Humphreys
ATTN: Code A353, S. Chappell
ATTN: Code A361, J. French
ATTN: Code A347, J. Mayo-Wells

NATO School, SHAPE
ATTN: US Documents Officer

DEPARTMENT OF ENERGY CONTRACTORS

University of California
Lawrence Livermore National Lab
ATTN: L-156, R. Kalibjian
ATTN: L-13, D. Meeker
ATTN: W. Orvis
ATTN: L-10, H. Kruger
ATTN: Tech Info Dept, Library
ATTN: L-156, J. Yee

Los Alamos National Lab
ATTN: J. Freed
ATTN: D. Lynn
ATTN: D. Wilde
ATTN: MS D450, B. McCormick
ATTN: C. Spirio

Sandia National Labs
ATTN: Div 2143, H. Weaver
ATTN: Org 2321, L. Posey
ATTN: Org 2150, J. Hood
ATTN: Div 2144, W. Dawes
ATTN: Div 2143, H. Sander
ATTN: Div 1232, G. Baldwin
ATTN: Org 2320, J. Renken
ATTN: Org 2100, B. Gregory
ATTN: T. Wrobel

DEPARTMENT OF DEFENSE CONTRACTORS

Advanced Rsch & Applications Corp
ATTN: R. Armistead
ATTN: T. Magee
ATTN: L. Palkuti

Advanced Rsch & Applications Corp
ATTN: A. Larson

Aerojet Electro-Systems Co
ATTN: D. Toomb
ATTN: SV/8711/70
ATTN: D. Huffman
ATTN: P. Lathrop

Aerospace Corp
ATTN: G. Gilley
ATTN: R. Crolius
ATTN: S. Bower
ATTN: W. Kolasinski, MS/259
ATTN: J. Stoll
ATTN: R. Slaughter
ATTN: B. Blake
ATTN: J. Wiesner
ATTN: J. Reinheimer
ATTN: C. Huang
ATTN: D. Fresh
ATTN: H. Phillips
ATTN: D. Schmunk
ATTN: P. Buchman
ATTN: V. Josephson, MS-4-933
ATTN: W. Crane, A2/1083
ATTN: I. Garfunkel
ATTN: A. Carlan

Aerospace Industries Assoc of America, Inc
ATTN: S. Siegel

Allied Corp
ATTN: Doc Con

Ampex Corp
ATTN: J. Smith
ATTN: D. Knutson

Analytic Services, Inc
ATTN: A. Shostak
ATTN: J. O'Sullivan
ATTN: P. Szymanski

AVCO Systems Div
ATTN: D. Fann
ATTN: C. Davis
ATTN: D. Shrader
ATTN: W. Broding

Battelle Memorial Institute
ATTN: R. Thatcher

BDM Corp
ATTN: C. Stickley
ATTN: S. Meth

BDM Corp
ATTN: D. Wunsch
ATTN: Marketing
ATTN: R. Antinone

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Beers Associates, Inc
ATTN: B. Beers
ATTN: S. Ives

Bendix Corp
ATTN: E. Meeder

Boeing Co
ATTN: R. Caldwell
ATTN: 8K-38
ATTN: D. Egelkrout
ATTN: H. Wicklein

Boeing Co
ATTN: MS-81-36, P. Blakely
ATTN: C. Dixon
ATTN: MS-2R-00, C. Rosenberg
ATTN: MS-81-36, W. Doherty
ATTN: MS-2R-00, A. Johnston
ATTN: MS-2R-00, I. Arimura
ATTN: C. Mulkey
ATTN: MS-2R-00, E. Smith

Booz, Allen & Hamilton, Inc
ATTN: R. Chrisner

California Institute of Technology
ATTN: P. Robinson
ATTN: K. Martin
ATTN: W. Price, MS-83-122
ATTN: D. Nichols, T-1180
ATTN: W. Scott
ATTN: R. Covey
ATTN: A. Shumka
ATTN: J. Coss
ATTN: F. Grunthaner

Charles Stark Draper Lab, Inc
ATTN: W. Callender
ATTN: Tech Library
ATTN: P. Greiff
ATTN: N. Tibbetts
ATTN: R. Ledger
ATTN: D. Gold
ATTN: R. Bedingfield
ATTN: R. Haltmaier
ATTN: A. Freeman
ATTN: J. Boyle

Cincinnati Electronics Corp
ATTN: L. Hammond
ATTN: C. Stump

Computer Sciences Corp
ATTN: A. Schiff

Control Data Corp
ATTN: T. Frey
ATTN: D. Newberry, BRR 142

University of Denver
ATTN: Sec Officer for F. Venditti

Dikewood Corp
ATTN: Tech Library for D. Pirio

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

E-Sytems, Inc
ATTN: K. Reis

E-Systems, Inc
ATTN: Div Library

Eaton Corp
ATTN: R. Bryant
ATTN: A. Anthony

Electronic Industries Assoc
ATTN: J. Kinn

University of Florida
ATTN: H. Sisler

FMC Corp
ATTN: M. Pollock, Mail Drop 080

Ford Aerospace & Comms Corp
ATTN: H. Linder
ATTN: Tech Info Svcs
ATTN: J. Davison

Franklin Institute
ATTN: R. Thompson

Garrett Corp
ATTN: H. Weil

General Dynamics Corp
ATTN: O. Wood
ATTN: R. Fields, MZ 2839

General Electric Co
ATTN: D. Tasca
ATTN: Tech Info Ctr for L. Chasen
ATTN: J. Peden
ATTN: J. Palchefsky, Jr
ATTN: Tech Library
ATTN: R. Benedict
ATTN: J. Andrews
ATTN: R. Casey

General Electric Co
ATTN: B. Flaherty
ATTN: L. Hauge
ATTN: G. Bender
ATTN: J. Reidl

General Electric Co
ATTN: G. Gati, MD-E184

General Electric Co
ATTN: D. Cole
ATTN: C. Hewison
ATTN: J. Gibson

General Elctric Co
ATTN: D. Pepin

General Rsch Corp
ATTN: A. Hunt

Goodyear Aerospace Corp
ATTN: Sec Con Station

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Grumman Aerospace Corp
ATTN: J. Rogers

GTE Comms Products Corp
ATTN: L. Blaisdell
ATTN: L. Pauplis
ATTN: W. Dunnet

GTE Comms Products Corp
ATTN: H. Ullman
ATTN: H&V Group
ATTN: P. Fredickson

GTE Comms Products Corp
ATTN: C. Thornhill
ATTN: J. Waldron
ATTN: C. Ramsbottom

Harris Corp
ATTN: W. Aeare
ATTN: E. Yost
ATTN: C. Davis

Harris Corp
ATTN: C. Anderson
ATTN: J. Cornell
ATTN: Mngr Bi-Polar Digital Eng
ATTN: T. Sanders. MS-51-121
ATTN: J. Schroeder
ATTN: Mgr Linear Engrg
ATTN: B. Gingerich, MS-51-120
ATTN: D. Williams, MS-51-75

Hazeltine Corp
ATTN: J. Okrent
ATTN: C. Meinen

Honeywell, Inc
ATTN: R. Gumm
ATTN: D. Nielsen, MN 14-3015
ATTN: F. Hampton
ATTN: J. Moylan

Honeywell, Inc
ATTN: H. Noble
ATTN: J. Schafer
ATTN: MS 725-5
ATTN: C. Cerulli
ATTN: J. Zawacki
ATTN: R. Reinecke

Honeywell, Inc
ATTN: Tech Library

Honeywell, Inc
ATTN: L. Lavoie

Honeywell, Inc
ATTN: D. Herold, MS-MN 17-2334
ATTN: R. Belt, MS-MN 17-2334
ATTN: D. Lamb, MS-MN 17-2334

Hughes Aircraft Co
ATTN: D. Binder
ATTN: CTDC 6/E110
ATTN: K. Walker
ATTN: R. McGowan

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Hughes Aircraft Co
ATTN: E. Smith, MS V347
ATTN: W. Scott, S32/C332
ATTN: A. Narevsky, S32/C332
ATTN: D. Shumake
ATTN: E. Kubo

Hughes Aircraft Co
ATTN: R. Henderson

Hughes Aircraft Co
ATTN: MS-A2408, J. Hall
ATTN: P. Coppen

IBM Corp
ATTN: Electromagnetic Compatability
ATTN: H. Mathers
ATTN: Mono Memory Systems
ATTN: T. Martin

IBM Corp
ATTN: J. Ziegler

IBM Corp
ATTN: N. Haddad
ATTN: A. Edenfeld
ATTN: H. Kotecha
ATTN: W. Henley
ATTN: MS 110-036, F. Tietze
ATTN: L. Rockett, MS 110-020
ATTN: O. Spencer
ATTN: S. Saretto
ATTN: W. Doughten

IIT Rsch Institute
ATTN: I. Mindel
ATTN: R. Sutkowski

IRT Corp
ATTN: N. Rudie
ATTN: R. Judge
ATTN: Physics Div
ATTN: MDC
ATTN: Systems Effects Div
ATTN: M. Rose
ATTN: J. Harrity
ATTN: R. Mertz

ITT Corp
ATTN: Dept 608
ATTN: A. Richardson

JAYCOR
ATTN: R. Stahl
ATTN: L. Scott
ATTN: R. Berger
ATTN: T. Flanagan
ATTN: J. Azarewicz
ATTN: M. Treadaway

JAYCOR
ATTN: R. Sullivan
ATTN: E. Alcaraz

JAYCOR
ATTN: C. Rodgers

Institute for Defense Analyses
ATTN: Tech Info Svcs

DEPARTMENT OF DEFENSE CONTRACTORS (CONTINUED)

JAYCOR
ATTN: R. Poll

Johns Hopkins University
ATTN: R. Maurer
ATTN: P. Partridge

Johns Hopkins University
ATTN: G. Masson, Dept of Elec Engr

Kaman Sciences Corp
ATTN: N. Beauchamp
ATTN: W. Rich
ATTN: J. Erskine
ATTN: C. Baker
ATTN: Dir Science & Technology Div

Kaman Sciences Corp
ATTN: E. Conrad

Kaman Tempo
ATTN: R. Rutherford
ATTN: DASIAC
ATTN: W. McNamara

Kaman Tempo
ATTN: DASIAC

Litton Systems, Inc
ATTN: F. Motter
ATTN: E. Zimmerman
ATTN: G. Maddox

Lockheed Missiles & Space Co, Inc
ATTN: F. Junga, S2/54-202
ATTN: J. Smith
ATTN: Reports, Library

Lockheed Missiles & Space Co, Inc
ATTN: B. Kimura
ATTN: G. Lum, Dept 81-63
ATTN: E. Hessee
ATTN: L. Rossi
ATTN: K. Greenough
ATTN: S. Taimuty, Dept 81-74/154
ATTN: J. Cayot, Dept 81-63
ATTN: P. Bene
ATTN: J. Lee
ATTN: G. Lum
ATTN: A. Borofsky, Dept 66-60, B/577N

LTV Aerospace & Defense Co
ATTN: Library
ATTN: R. Tomme
ATTN: Tech Data Ctr

M. I. T. Lincoln Lab
ATTN: P. McKenzie

Magnavox Advanced Products & Sys Co
ATTN: W. Hagemeier

Magnavox Govt & Indus Electronics Co
ATTN: W. Richeson

McDonnell Douglas Corp
ATTN: Tech Library

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Martin Marietta Corp
ATTN: MP-163, W. Bruce
ATTN: R. Gaynor
ATTN: H. Cates
ATTN: S. Bennett
ATTN: J. Ward
ATTN: MP-163, N. Redmond
ATTN: J. Tanke
ATTN: P. Fender
ATTN: R. Yokomoto
ATTN: W. Janocko
ATTN: TIC/MP-30
ATTN: W. Brockett

Martin Marietta Denver Aerospace
ATTN: D-6074, G. Freyer
ATTN: M. Shumaker
ATTN: Rsch Library
ATTN: Goodwin
ATTN: P. Kase
ATTN: MS-D6074, M. Polzella

McDonnell Douglas Corp
ATTN: Library
ATTN: A. Munie
ATTN: M. Stitch, Dept E003
ATTN: T. Ender, 33/6/618
ATTN: D. Dohm
ATTN: R. Kloster, Dept E451

McDonnell Douglas Corp
ATTN: R. Lothringer
ATTN: D. Fitzgerald
ATTN: P. Albrecht
ATTN: M. Onoda
ATTN: J. Holmgrem
ATTN: J. Imai
ATTN: P. Bretch
ATTN: M. Ralsten

Mission Rsch Corp
ATTN: C. Longmire
ATTN: M. Van Blaricum

Mission Rsch Corp
ATTN: D. Merewether
ATTN: R. Turfler
2 cy ATTN: D. Alexander
2 cy ATTN: R. Pease

Mission Rsch Corp
ATTN: J. Lubell
ATTN: W. Ware
ATTN: R. Curry

Mission Rsch Corp, San Diego
ATTN: J. Raymond
ATTN: V. Van Lint

Mitre Corp
ATTN: M. Fitzgerald

Motorola, Inc
ATTN: A. Christensen

Motorola, Inc
ATTN: C. Lund
ATTN: L. Clark
ATTN: O. Edwards

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

National Academy of Sciences
ATTN: National Materials Advisory Brd

National Semiconductor Corp
ATTN: F. Jones
ATTN: J. Martin
ATTN: A. London

New Technology, Inc
ATTN: D. Divis

Norden Systems, Inc
ATTN: D. Longo
ATTN: Tech Library

Northrop Corp
ATTN: J. Srour
ATTN: A. Bahraman
ATTN: S. Othmer
ATTN: P. Eisenberg
ATTN: Z. Shanfield
ATTN: A. Kalma

Northrop Corp
ATTN: P. Gardner
ATTN: S. Stewart
ATTN: E. King, C3323/WC
ATTN: T. Jackson
ATTN: L. Apodaca

Pacific-Sierra Rsch Corp
ATTN: H. Brode, Chairman SAGE

Palisades Inst for Rsch Svcs, Inc
ATTN: Secretary

Physics International Co
ATTN: J. Shea
ATTN: Div 6000

R&D Associates
ATTN: W. Karzas
ATTN: P. Haas

Rand Corp
ATTN: C. Crain
ATTN: P. Davis

Rand Corp
ATTN: B. Bennett

Raytheon Co
ATTN: T. Wein
ATTN: J. Ciccio
ATTN: G. Joshi

Raytheon Co
ATTN: A. Van Doren
ATTN: H. Flescher

RCA Corp
ATTN: V. Mancino
ATTN: G. Brucker

RCA Corp
ATTN: R. Killian

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

RCA Corp
ATTN: D. O'Connor
ATTN: R. Smeltzer
ATTN: G. Hughes
ATTN: Office, N103
ATTN: L. Minich
ATTN: L. Napoli

RCA Corp
ATTN: L. Debacker
ATTN: E. Schmitt
ATTN: W. Allen

RCA Corp
ATTN: R. Magyarics
ATTN: J. Saultz
ATTN: E. Van Keuren
ATTN: W. Heagerty

Rensselear Polytechnic Institute
ATTN: R. Gutmann
ATTN: R. Ryan

Research Triangle Institute
ATTN: M. Simons

Rockwell International Corp
ATTN: A. Rovell
ATTN: V. Strahan
ATTN: V. Michel
ATTN: J. Bell
ATTN: R. Pancholy
ATTN: J. Pickel, Code 031-BB01
ATTN: V. De Martino
ATTN: C. Kleiner
ATTN: GA50 TIC/L, G. Green
ATTN: K. Hull
ATTN: J. Blandford

Rockwell International Corp
ATTN: TIC D/41-092, AJ01
ATTN: D. Stevens

Rockwell International Corp
ATTN: TIC 124-203
ATTN: L. Pinksto[illegible], 106-183

Rockwell International Corp
ATTN: TIC BA08
ATTN: T. Yates

Sanders Assoc, Inc
ATTN: L. Brodeur

Science Applications, Inc
ATTN: D. Long
ATTN: J. Retzler
ATTN: D. Strobel
ATTN: R. Fitzwilson
ATTN: J. Spratt
ATTN: L. Scott
ATTN: D. Millward
ATTN: J. Naber
ATTN: J. Beyster
ATTN: V. Verbinski
ATTN: V. Orphan

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Science Applications, Inc
ATTN: J. Wallace
ATTN: W. Chadsey

Science Applications, Inc
ATTN: D. Stribling

Scientific Rsch Assoc, Inc
ATTN: H. Grubin

Singer Co
ATTN: J. Brinkman
ATTN: J. Laduca
ATTN: R. Spiegel
ATTN: Tech Info Ctr

Sperry Corp
ATTN: Engrg Lab

Sperry Corp
ATTN: J. Inda

Sperry Corp
ATTN: R. Viola
ATTN: F. Scaravaglione
ATTN: P. Maraffino
ATTN: C. Craig

Sperry Flight Systems
ATTN: D. Schow

SRI International
ATTN: A. Whitson

SRI International
ATTN: A. Padgett

Sundstrand Corp
ATTN: Rsch Dept

System Development Corp
ATTN: Product Evaluation Lab

Systron-Donner Corp
ATTN: J. Indelicato

Teledyne Brown Engrg
ATTN: B. Hartway
ATTN: D. Guice

TRW Electronics & Defense Sector
ATTN: H. Holloway
ATTN: W. Willis
ATTN: H. Hennecke
ATTN: P. Reid, MS R6/2541
ATTN: H. Volmerange, R1/1126
ATTN: A. Witteles, MS R1/2144
ATTN: R. Von Hatten
ATTN: P. Guilfoyle
ATTN: F. Friedt
ATTN: R. Kingsland
ATTN: Tech Info Ctr
ATTN: W. Rowan
ATTN: D. Clement
ATTN: Vulnerability & Hardness Lab
ATTN: M. Ash
2 cy ATTN: O. Adams
2 cy ATTN: R. Plebuch

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Teledyne Systems Co
ATTN: R. Suhrke

Texas Instruments, Inc
ATTN: R. McGrath
ATTN: D. Manus
ATTN: E. Jeffrey, MS 961
ATTN: T. Cheek, MS 3143
ATTN: R. Carroll, MS 3143
ATTN: F. Poblenz, MS 3143
ATTN: R. Stehlin

Westinghouse Electric Corp
ATTN: S. Wood

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

TRW Electronics & Defense Sector
ATTN: J. Gorman
ATTN: F. Fay
ATTN: C. Blasnek
ATTN: R. Kitter

Westinghouse Electric Corp
ATTN: H. Kalapaca, Ms 3330
ATTN: L. McPherson
ATTN: E. Vitek, MS 3200
ATTN: MS 3330
ATTN: MS 330, D. Grimes
ATTN: J. Cricchi
ATTN: N. Bluzer

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